Code No: 09A50402 **R09** **Set No. 2**

III B.Tech I Semester Examinations,December 2011
COMPUTER ORGANIZATION
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Discuss in detail inter processor arbitration logics and procedures with necessary diagrams? [15]

2. (a) Discuss asynchronous serial transfer concept?
   (b) Explain in detail control field format in bit oriented protocol? [7+8]

3. (a) List and explain various categories of computers in Flynn's Classification.
   (b) Describe operand forwarding techniques in detail. [7+8]

4. (a) Explain a 4 bit binary incremented?
   (b) Describe the Execution of register reference instructions? [7+8]

5. (a) For the hexadecimal main memory addresses 111111, 666666, BBBBBB. Show the following information in hexadecimal format.
      i. Tag, Line and Word values for a direct mapped cache.
      ii. Tag set and word values for a two way set associative cache.
   (b) Explain CD technology and variants of CD disks. [7+8]

6. (a) What are the major design considerations in microinstruction sequencing? Explain?
   (b) Discuss microinstruction sequencing techniques, specifically variable format address microinstruction. [8+7]

7. (a) Convert the decimal numbers to bases indicated
      i. 7562 to Octal
      ii. 1947 to Hexadecimal.
   (b) Explain various buses such as internal, external, backplane, I/O, system, address, data, synchronous and Asynchronous. [5+10]

8. Design an array multiplier that multiplies two 4- bit numbers using binary adders and AND gates. [15]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 09A50402 **R09** **Set No. 4**

III B.Tech I Semester Examinations,December 2011
COMPUTER ORGANIZATION
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Write a note on Stack operations?
   (b) List some data transfer instruction and explain with examples? [5+10]
2. Derive the circuits for a 4 bit parity generator and 5 bit parity checker using an EVEN parity bit. [15]
3. Explain designing of control unit in detail with necessary block diagrams? [15]
4. (a) Explain the operation of crossbar switch networks with neat diagram?
   (b) Discuss in detail parallel arbitration logic for multi processor system? [7+8]
5. (a) What differences between a CD and a DVD account for the larger capacity of the lattee?
   (b) List and explain various types of ROM. [7+8]
6. (a) Give an example that uses delayed load with the three segment pipeline?
   (b) Discuss in detail the applications of vector processing? [7+8]
7. Derive an algorithm in flowchart for the non restoring method of fixed point binary division. [15]
8. A DMA controller transfer 16 bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per seconds. By how much will the CPU be slowed down because of the DMA transfer? Explain Your answer? [15]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 09A50402 **R09** **Set No. 1**

III B.Tech I Semester Examinations,December 2011
COMPUTER ORGANIZATION
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Briefly explain arithmetic logic shift unit with help of a functional table? [15]
2. Explain direct memory access transfer in a computer system? [15]
3. What is vector processing? List its application and explain matrix multiplication with an example. [15]
4. (a) How many switch points are there in a crossbar switch network that connects 'P' processors to 'm' memory modules? Give a neat sketch?
   (b) Discuss inter process synchronizations? [7+8]
5. Divide -145 by 13 in binary 2's complement notation, using 12 - bit words. Explain division process with necessary algorithm.
6. What is meant by writable control memory? Explain micro program control organization with necessary diagrams. [15]
7. (a) A two way set associative cache has lines of 16 bytes and a total size of 8 k bytes. The 64 Mbytes main memory is byte addressable. Show the format of main memory address.
   (b) Discuss about DVD technology. [7+8]
8. (a) Obtain the 1's and 2's complement of the following:
      i. 10101110
      ii. 10000001
      iii. 10000000
      iv. 10101010.
   (b) List the Functions need to the performed by system software? [15]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 09A50402 **R09** **Set No. 3**

III B.Tech I Semester Examinations,December 2011
COMPUTER ORGANIZATION
Common to Electronics And Telematics, Electronics And Communication Engineering

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Describe the following terminology associated with multi processors
   (a) Mutual exclusion.
   (b) Hardware lock.
   (c) Semaphore.
   (d) Test and set instruction. [15]
2. Discuss the features of dynamic microprogramming in detail. [15]
3. (a) List and explain the SCSI bus signals.
   (b) Explain in detail destination initiated transfer using handshaking method. [7+8]
4. (a) Give an example that uses delayed branch with the three segment pipeline?
   (b) Give a detail note on attached array processor? [7+8]
5. (a) Let register A holds the 8 bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to :
      i. 01101101
      ii. 11111101
   (b) What is a stack? Explain push and pop instructions using stack with examples? [7+8]
6. Multiply 32 by 18 using Booth algorithm and explain step by step process. [15]
7. (a) Give the 2's complement notation for the following signed decimal numbers for 8 bit word
      i. +1
      ii. +127
      iii. -1
      iv. -64.
   (b) Write a detail note on Bus Structures? [7+8]

8. Consider a single level cache with an access time of 2.5ns, a line size of 64 bytes, and a hit ratio of H= 0.95. Main memory uses a block transfer capability that has a first word (4 bytes) access time of 15ns and an access time of 5ns for each word there after.

   (a) What is the access time when there is a cache miss? Assume that the cache waits until the line has been fetched from main memory and then re executes for a hit?

   (b) Suppose that increasing the line size to 128bytes increases the H to 0.97. Does this reduce the average memory access time? Justify your answer. [7+8]

⋆ ⋆ ⋆ ⋆ ⋆