Code No: 07A4EC13 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY HYDERABAD
II B.Tech.II Sem. II Mid-Term Examinations, April – 2009
COMPUTER ORGANIZATION
Objective Exam
Name: _____ Hall Ticket No. _____
Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternate:

1. Machines whose instructions generate 32-bit address can utilize a memory that contains up to _____ memory locations. [ ]
   A. 2^8 B. 2^{16} C. 2^{32} D. 2^{48}

2. An important feature for PCI is a _____ capability for I/O devices [ ]
   A. Switch and connections B. Plug and Play C. Inter Connection D. Inter Networking

3. The speed up of a pipeline processing over an equivalent non-pipeline processing is defined by the ratio S =_____ [ ]
   A. $nt_n /(k+n-1)t_p$ B. $nt_p/(k+n-1)t_n$ C.$nt_n /(k+n+1)t_p$ D.$nt_p/(k-n-1)t_n$

4. The _____ organization consists of a number of cross points that are placed at intersections between processors buses and memory module paths. [ ]
   A. Multiport memory B. Hypercube system
   C. Crossbar Switch D. Time –shared common bus

5. The minimum time delay required between the initiations of two successive memory operations. [ ]
   A. Memory access time B. Seek time C. Latency time D. Memory Cycle time

6. The CPU has distinct i/p and o/p instructions and each of these instructions is associated with the address of an interface register. [ ]
   A. Memory Mapped I/O B. I/O Port C. Isolated I/O D. I/O Command

7. Application of Vector Processing is [ ]
   A. Library System B. Medical Diagnosis C. Seismic Wave Analysis D. Space Research

8. Non shared and read –only data to be stored in caches is called as [ ]
   A. Cachable B. Non Cachable C. Cache Coherence D. Cache Inc coherence

9. An _____ is an auxiliary processor attached to a general purpose computer . [ ]
   A. SIMD array Processor B. Attached array Processor C. Vector Processor D. All the above

10. Backup storage is called as [ ]
    A. Cache Memory B. Main Memory C. Auxiliary Memory D. Virtual Memory

Cont…2

II Fill in the blanks

11. Meaning of NAK _____

12. The number of hits stated as a fraction of all attempted accesses is called _____

13. In an_____ different sets of addresses are assigned to different memory locations.

14. The bus grant signal is replaced by a set of lines called poll lines which are connected to all units is called as _____.

15. Expand MFC _____.

III True or False Statements

16. In CISC architecture, instructions that manipulate operands in memory? [True/False]

17. Hardware interlocks uses special hardware to detect a conflict and then avoid it by routing the data through special paths between pipeline segments. [True/False]

18. Simplex line carries information in both directions? [True/False]

19. In non pipeline unit that performs same operation and takes a time equal to t_n to complete each task. The total time required for n tasks is nt_p . [True/False]

20. Data dependency conflicts arise when an instruction depends on the result of a previous instruction, but this result is not yet available. [True/False]

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Code No: 07A4EC13 **Set No. 2**

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COMPUTER ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternate:

1. Baud rate is data transfer in [ ]
   A.bits per second B. bytes per second C. words per second D. all the above

2. 64-Mbit chip may be organized [ ]
   A.16M×4 B. 8M×8 C. 4M×16 D. all the above

3. An _____is a processor that as single instruction multiple data organization [ ]
   A. SIMD array Processor B. Attached array Processor C. Vector Processor
   D. All the Above.

4. The binary n-cube multiprocessor structure is a loosely coupled system Composed of _____ processors interconnected in an _____ dimensional binary cube. [ ]
   A. $N= 2^{n+1}$, n+1 B. $N= 2^{n}$, n C. $N= 2^{n-1}$, n-1 D. $N=2^{n}$, n+1

5. Data transfer to and from peripherals may be handled [ ]
   A. Programmed-I/O B. Interrupted-Initiated I/O
   C. Direct Memory Access D. all the above

6. During a _____ operation, the sense/read circuits, the information stored in the cells selected by a word line and transmit this information to the o/p data lines [ ]
   A. Write B. Read C. Read/Write D. Write & Read/Write

7. To compute n-tasks using a k-segments pipeline requires _____ clock cycles [ ]
   A. k-(n+1) B. k-(n-1) C. k+ (n-1) D. k+ (n+1)

8. The _____ algorithm allocates a fixed –length time slice of bus time that is offered sequentially to each processor. [ ]
   A. FIFO B. LRU C. Time slice D. Polling

9. Super computers are _____ [ ]
   A. Very Powerful B. High- Performance
   C. Less Expensive D. Both Very Powerful & High- Performance

10. Cells don't retain their state indefinitely_____ [ ]
    A. Static RAM'S B. Dynamic RAM'S C. SROM'S D. DROM'S

Cont…2

II Fill in the Blanks

11. Expand UART: _____

12. _____ is a technique of decomposing a sequential process into sub operations, with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

13. Let h be the hit rate, M the miss penalty, that is, the time to access information in the main memory, and c the time to access information in the cache. The average access time expressed by the process is t_{ave}=_____

14. In the _____ policy, both cache and main memory are updated with every write operation.

15. Input-Output interface provides a method for transferring information between _____ and _____

III True or False Statements

16. In non-vector Interrupt, the branch address is assigned to a fixed location. [True/False]

17. Character oriented protocol is HDLC and ADCCP. [True/False]

18. In content addressable memory, memory is accessed simultaneously and in parallel on the basis of data content rather by specific address or location. [True/False]

19. The physical memory is broken into groups of unequal size called blocks. [True/False]

20. In a vector interrupt, the source that interrupts supplies the branch information to the computer. [True/False]

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Code No: 07A4EC13 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY HYDERABAD
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COMPUTER ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternate:

1. The time that elapses between the initiation of an operation and the completion of that operation . [ ]
   A. Memory access time B. Seek time C. Latency time D. Memory Cycle time

2. The interface transfer s data into and out of the memory unit through the memory bus. [ ]
   A. Programmed-I/O B. Interrupted-Initiated I/O C. Direct Memory Access D. all the above

3. _____ arise from branch and other instructions that change the value of pc [ ]
   A. Data Dependency B. Resource conflict C. Branch difficulties D. NONE

4. Shared writable data are [ ]
   A. Cachable B. Non Cachable C. Cache Coherence D. Cache Inc coherence

5. Examples of bit-oriented protocols are [ ]
   A. SDLC B. HDLC C. ADCCP D. all the above

6. The amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head [ ]
   A. Rotational delay B. latency time
   C. seek time D. Both Rotational delay & latency time

7. An _____ operates on a stream of instructions by overlapping the fetch, decode and execute phases of the instruction cycle. [ ]
   A. Arithmetic pipeline B. Instruction Pipeline
   C. Pipelining D. Arithmetic pipeline & Instruction Pipeline

8. In the _____ only the cache is updated and the location is marked so that it can be copied later into main memory. [ ]
   A. Write through policy B. Cache Coherence C. Write- back policy D. Cache Incoherence

9. Which type of array processor manipulate vectors, their internal organization is different. [ ]
   A. SIMD array Processor B. Attached array Processor
   C. Vector Processor D. SIMD array Processor & Attached array Processor

10. Transfer of data is between CPU and peripheral is called as [ ]
    A. Programmed-I/O B. Interrupted-Initiated I/O C. Direct Memory Access D. all the above

Cont…2

II Fill in the Blanks

11. During _____operation, the sense/Write circuit receive input information and store it in the cells of the selected word.

12. The DMA controller to transfer one data word at a time, after which it must return control of the buses to the cpu, this technique is called as _____.

13. The sequence of instructions read from memory is s called as_____

14. A _____ is a program sequence that, once begun, must complete execution before another processor access the same shared resource.

15. Expand SIMD_____

III Match the following

16) TSL	[	]	P) Shared- memory
17) Tightly coupled multi processor	[	]	Q) test and set while locked
18) Loosely coupled multi processor	[	]	R) Auxiliary memory
19) Very high speed memory	[	]	S) Distributed –memory
20) Magnetic disks	[	]	T) Cache –memory

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Code No: 07A4EC13 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY HYDERABAD
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Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternate:

1. There are 20 data recording surface with 15,000 tracks per surface .There is an average of 400 sectors per track and each sector contain 512 bytes of data. Hence total capacity of the formatted disk is (GB=giga bytes, MB= mega bytes) [ ]
   A. 40 MB B. 60 MB C. 40 GB D. 60 GB

2. Function of SOH [ ]
   A. Establishes synchronism B. Heading of block message
   C. Precedes block of text D. concludes transmission

3. _____ caused by access to memory by two segments at the same time [ ]
   A. Data dependency B. Resource Conflict C. Branch difficulties D. Delay load

4. The _____algorithm gives the highest priority to the requesting device that has not used the bus for the longest interval. [ ]
   A. Round - robin B.FIFO C. LRU D. rotating daisy-chain

5. Many instructions in localized areas of the program are executed repeatedly during some time period, and the remainder of the program is accessed relatively infrequently. [ ]
   A. Locality reference B. spatial C. temporal D. cache

6. The _____ is specified by the CPU to indicate the type of operation required from the IOP. [ ]
   A. CAR B. CCW C. DCP D. DMA

7. Multi processors and Multi computer system come into which category [ ]
   A. MIMD B. SIMD C. SISD D. MISD

8. The exchange of data between different processes [ ]
   A. Inter lock B. Hardware lock C. Communication D. Inter lock & Hardware lock

9. A _____ transmission can send and receive data in both directions simultaneously [ ]
   A. Simplex B. Full duplex C. Half Duplex D. Simplex & Full duplex

10. Memories that consist of circuits capable of retaining their state as long as power is applied are known as ____ [ ]
    A. Main Memory B. Cache Memory C. Static Memory D. Dynamic Memory

Cont…2

II Fill in the Blanks

11. Disks that are permanently attached to the unit assembly and cannot be removed by the occasional user are called as_____.

12. The communication lines, modems, and other equipment used in the transmission of information between two or more stations is called a_____

13. Expand PCI :_____

14. An address generated by the processor is referred as_____

15. Expand LRC:_____

III True or False Statements

16. A half duplex transmission system is one that is capable of transmitting in both directions but data can be transmitted in only one direction? [True/False]

17. Control command is issued to activate the peripheral and to inform it what to do? [True/False]

18. Flynn's classification is divides computers into three major groups? [True/False]

19. RISC architecture uses inefficient instruction pipeline? [True/False]

20. An interlock is a circuit that detects instructions whose source operand are destination of instructions further up in the pipeline? [True/False]

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