Code No: 05210505 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem. II Mid-Term Examinations, April – 2009

COMPUTER ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative

1. The speed imbalance between memory access and CPU operation can be reduced by [ ]
   A) Cache memory B) Memory interleaving C) Reducing the size of memory
   D) Increasing the size of memory

2. A computer with a 32-bit wide data bus uses 4Kx8 static RAM memory chips. The smallest memory this computer can have is [ ]
   A) 32kb B) 16kb C) 8kb D) 25kb

3. Which of the following is volatile? [ ]
   A) Bubble memory B) RAM C) ROM
   D) Magneticdisk

4. What is the correct sequence of time delays that happen during a data transfer from a disk to memory? [ ]
   A) Seek time, access time, transfer time B) Seek time, latency time, transfer time
   C) Latency time, seek time, transfer time D) Latency time, access time, transfer time

5. In a non-vectored interrupt [ ]
   A) The branch address is assigned to a fixed location in memory
   B) The interrupting source supplies the branch information to the processor through an interrupt vector
   C) The branch address is obtained from a register in the process
   D) Both The interrupting source supplies the branch information to the processor through an interrupt vector & The branch address is obtained from a register in the process

6. A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. What is the maximum speed up that can be achieved? [ ]
   A) 6 B) 5 C) 4 D) 2

7. A pipeline has the following propagation times: 40ns for the operands to be read into registers R1 & R2, 45ns for the signal to propagate through the multiplier, 5ns for the transfer into R3, and 15ns to add the two numbers into R5. What is the minimum clock cycle time that can be used?[ ]
   A) 45 B) 5 C) 50 D) 105

Cont…..2

Code No: 05210505 **Set No. 1**

8. A technique of decomposing a sequential process into sub operations, with each sub process being executed in a special dedicated segment that operates concurrently with all other segments is called [ ]
   A) Pipeline processing B) Vector processing
   C) Array processing D) Sequential processing

9. One transfer at a time is a characteristic of [ ]
   A) Timeshared common bus B) jcross bar switch C) Hypercube system
   D) Multiport memory

10. If here are n CPUs and m memory modules, the number of switches required in crossbar switch configuration is [ ]
    A) m+n B) mn C) m/n D) m-n

II Fill in the blanks

11. The mode of transfer in which the CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer is called _____

12. A hyper cube with 2-dimensions contain _____ number of processors.

13. The associative memory used to hold the most recently referenced table entries in virtual memory is called _____

14. Acronym for RAID stands for _____

15. An 8x8 omega switching network contains _____ number of switches

III True or False Statement

16. In the isolated I/O configuration, the CPU has distinct input and output instructions. [True/False]

17. In a microprocessor system using I/O mapped I/O, I/O and memory address space are distinct [True/False]

18. Bootstrap loader is stored in RAM [True/False]

19. Time-slice algorithm is a dynamic arbitration algorithm [True/False]

20. SDLC is a bit-oriented protocol for serial communication [True/False]

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Code No: 05210505 **Set No. 2**

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III B.Tech. II Sem. II Mid-Term Examinations, April – 2009

COMPUTER ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative

1. A byte addressable computer has a memory capacity of 2^m K bytes and can perform 2^n operations. An instruction involving three operands and one operator needs a maximum of [ ]
   A) 3m bits B) 3m+n bits C) m+n bits D)3m+n+30

2. FFFF will be the last memory location in a memory of size [ ]
   A) 1K B) 16K C) 32K D) 64K

3. The cost for storing a bit is minimum in [ ]
   A) Cache B) Register C) RAM D) Magnetic tape

4. The memory which is programmed at the time it is manufactured is [ ]
   A) ROM B) RAM C) PROM D) EPROM

5. A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed-up ratio of the pipeline for 100 tasks. [ ]
   A) 500/109 B) 6 C) 1/5 D) 100/6

6. The time delay of the four segments in the pipeline is as follows: t1=50ns, t2=30ns, t3=95ns, and tn=45ns. The interface registers delay time tr=5ns. What is the minimum clock cycle time? [ ]
   A) 100 B) 55 C) 225 D) 105

7. The number of bits that are typically stored on each track of a magnetic disk is usually [ ]
   A) The same B) Different C) Depend on the program to be stored
   D) Fifty

8. Multiprocessors are classified as [ ]
   A) MIMD B) MISD C) SIMD D) SISD

9. A hyper cube of 3-dimensions contains _____ number of processors [ ]
   A) 3 B) 2^3 C) 3^2 D) 3+3

Cont….2

Code No: 05210505 **Set No. 2**

10. The overall transfer rate with in the system is less in [ ]
    A) Time-shared common bus B) Multiport memory
    C) Crossbar switch D) Hypercube system

II Fill in the blanks

11. Acronym UART stands for _____

12. The mode of transfer in which the data into and out of the memory unit is transferred through the memory bus is called _____

13. An nxn omega switching network contains _____

14. Virtual memory is the concept that permits the user to construct programs as though a large memory equal to _____

15. _____ is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a special dedicated segment that operates concurrently with all other segments.

III True or False Statements

16. Memory mapped IO system employs same set of read and write signals for memory and IO [True/False]

17. A bit-oriented protocol for serial communication works only for ASCII text [True/False]

18. DMA causes memory consistency problems [True/False]

19. Multiprocessor is a tightly coupled system [True/False]

20. For a microprocessor system using IO mapped IO, I/O address space is greater [True/False]

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Code No: 05210505 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem. II Mid-Term Examinations, April – 2009

COMPUTER ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative

1. A word addressable computer with the word size being 8 bytes has a memory capacity of 2^mKBytes and can perform 2^n operations. An instruction involving 3 operands and one operator needs a maximum of [ ]
   A) 3m bits B) 3m+n bits C) m+n bits D) 3m+n+24

2. If the cache needs an access time of 20ns and main memory 120ns, then the average access time of a CPU is (assume hit-ratio is 80%) [ ]
   A) 30ns B) 40ns C) 35ns D) 45ns

3. In a memory-mapped IO system, which of the following instruction will not be there? [ ]
   A) LDA B) ADD C) SUB D) OUT

4. In a virtual memory system, the address space specified by the address lines of the CPU must be _____ than the physical memory size, and _____ than the secondary storage size. [ ]
   A) Smaller, smaller B) Smaller, larger C) Larger, smaller D)Larger, larger

5. Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. [ ]
   A) 200 B) 205 C) 206 D) 6

6. A pipeline has the following propagation times: 40ns for the operands to be read from memory into registers R1 and R2, 45ns for the signal to propagate through the multiplier, 5ns for the transfer into R3, and 15ns to add the two numbers into R5. What is the maximum speed up that can be achieved? [ ]
   A) 4 B) 45 C) 3 D) 5

7. Von Neumann architecture is [ ]
   A) SISD B) SIMD C) MIMD D) MISD

Cont….2

Code No: 05210505 **Set No. 3**

8. When we move from the outmost track to the innermost track in a magnetic disk the density (bits/linear inch) [ ]
A) Increases B) Decreases C) Remains same D) Either remains constant or decreases

9. A hypercube with 4-dimensions contain _____ number of processors. [ ]
A) 16 B) 4 C) 8 D) 32

10. Bootstrap loader is stored in [ ]
A) ROM B) RAM C) Cache memory D) Hard-disk

II Fill in the blanks

11. The number of stages in nxn omega switching network is _____

12. Associative memory is called _____

13. _____is a device that converts digital signals to analog signals and vice-versa

14. A serial transmission technique which employs special bits to mark the ends of character is called _____

15. The acronym for DMA stands for _____

III True or False Statements

16. In a memory mapped IO organization, there are no specific input or output instructions [True/False]

17. In a non-vectored interrupt the branch address is assigned a fixed location [True/False]

18. Daisy-chaining priority is a software polling method [True/False]

19. Multiprocessor is loosely coupled system [True/false]

20. Memory protection is not possible with virtual memory [True/False]

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Code No: 05210505 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. II Sem. II Mid-Term Examinations, April – 2009
COMPUTER ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. _____

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative

1. If a memory access takes 20ns with cache and 110ns without it, then the hit ratio (cache uses a 10ns memory) [ ]
   A) 93% B) 90% C) 87% D) 88%

2. The seek time of a disk is 30ms. It rotates at the rate of 30 rotations per second. Each track has a capacity of 300 words. The access time is, approximately. [ ]
   A) 47ms B) 50ms C) 60ms D) 62ms

3. The number of RAM chips of size (256x1) required to build 1MByte memory is [ ]
   A) 8 B) 32 C) 10 D) 24

4. The capacity of a memory unit is defined in terms of the number of words multiplied by the number of bits/word. The number of separate address and data lines needed for a memory of 4Kx16 is [ ]
   A) 10,16 B) 11,8 C) 12,16 D) 12,12

5. In a system with 64-bit virtual addresses and 43-bit physical addresses, how many pages are there in virtual memory and physical memory if pages are 8KB in size. [ ]
   A) 2^{51} and 2^{30} B) 51 and 30 C) 2^{64} and 2^{43} D) 2^{13}and2^{13}

6. Suppose an un-pipelined processor with a 25ns cycle time is divided into 5 pipeline stages with processing time 5, 7, 3, 6 and 4ns. What is the cycle time of the resulting processor.[ ]
   A) 8 B) 7 C) 3 D) 5

7. Determine the number of clock cycles that it takes to process eight tasks in a six-segment pipeline [ ]
   A) 13 B) 14 C) 6 D) 8

8. An un-pipelined processor with a clock cycle t_n is divided into k-segment pipeline with a clock cycle t_p to execute n tasks. What is the speed up ratio? [ ]
   A) $nt_n/(k+n-1)t_p$ B) t_n/t_p C) t_p/t_n D) $(k+n-1)t_p/nt_n$

9. In comparison to the main memory, tape or disk memory is [ ]
   A) Slower and more expensive B) Slower and less expensive
   C) Faster and more expensive
   D) Faster and less expensive

Cont….2

Code No: 05210505 **Set No. 4**

10. Von Neumann architecture is [ ]
A) SISD B) SIMD C) MIMD D) MISD

II Fill in the blanks

11. _____is the concept that permits the user to construct programs as though a large memory equal to totality of auxiliary memory is available.

12. The number of switches in each stage of an nxn omega network is _____

13. A serial transmission in which the two units share a common clock is called _____transmission

14. If the branch address of the interrupt routine is supplied by the source it is called _____interrupt.

15. The phenomenon that the references to memory at any given interval of time tend to be confined with in a few localized areas is called _____

III True or False Statements

16. For a microprocessor system using IO mapped IO memory space available is greater. [True/False]

17. Using DMA transfer the available memory bandwidth for programs is reduced while DMA is occurring [True/False]

18. Multiprocessor is an MIMD architecture [True/False]

19. RISC uses an efficient instruction pipelining [True/False]

20. Bootstrap loader will usually be stored in RAM [True/False]

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