JNTU ONLINE EXAMINATIONS Computer Organization [CO]

1. Computer design is concerned with
a. The way hardware components operate and connected together to form Computer system.
b. The determination of what hardware should be used and how the parts be connected.
c. The structure and behavior of the computer as seen by the user.
d. Design of electronic components of computer.
2. A digital computer with more than one processor is called as
a. Multi Programming System
b. Multiprocessor System
c. Multitasking System
d. Multi Computer System
3. Computer Organization is concerned with
a. The way hardware components operate and connected together to form Computer system.
b. The determination of what hardware should be used and how the parts be connected.
c. The structure and behavior of the computer as seen by the user.
d. Design of electronic components of computer.
4. Computer architecture is concerned with
a. The way hardware components operate and connected together to form Computer system.
b. The determination of what hardware should be used and how the parts be connected.
c. The structure and behavior of the computer as seen by the user.
d. Design of electronic components of computer.
5. In a computer system control information is transferred in
a. address and data buses
b. address and control buses
c. address bus only
d. control bus only
6. The part of the hardware of computer that controls the transfer of information between computer and the outside word is
a. CPU
b. Memory
c. IOP
d. Microprocessor
7. The part of the hardware of computer that is used to manipulate data is
a. CPU
b. Memory
c. IOP
d. Microprocessor
8. The functional entity of computer system that does not have physical existence is
a. CPU
b. Hardware
c. Software
d. Logic gates.
9. Digital computers use

a. Decimal number system
b. Octal number system
c. Binary number system
d. Hexadecimal number system
10. A system software is
a. A program to solve particular problem of a user
b. A machine independent program
c. Operating system dependent program.
d. A program to make effective use of computer
11. Which of the following statement(s) is(are) correct?
a. Instructions in a stack-based organization take up less memory than general purpose register organization instructions.
b. Programming is easier with stack-based organization compared to general purpose register organization.
c. Programs tend to become shoter in stack-based organization compared to general purpose register organization.
d. Instructions in a stack- based organization take up more memory than general purpose register organization instructions.
12. Signed 1's complement representation of -14 with eight bits is
a. 11110001
b. 01110001
c. 10001110
d. 00001110
13. 2's complement representation of -32 with eight bits is
a. 01100000
b. 11100000
c. 00100000
d. 10010000
14. The 1' s complement of decimal number 21 in binary is
a. 01010
b. 10101
c. 11011
d. 10100
15. Signed 2's complement representation of +14 with eight bits is
a. 10001110
b. 11110010
c. 00001110
d. 11110001
16. 2's complement representation of 16 with eight bits is
a. 10001111
b. 11110010
c. 00001111
d. 00010000
17. **The complement of decimal number 85 is**
a. 84

b. 15
c. 14
d. 16
18. **The complement of decimal number 65 is**
a. 35
b. 34
c. 36
d. 66
19. The 1's complement of binary number 01011011 is
a. 11011011
b. 01100100
c. 10100100
d. 10111011
20. The 2's complement of binary number 01010001 is
a. 10101110
b. 10101111
c. 01001110
d. 01010010
21. Signed magnitude representation of -7 with eight bits is
a. 10000111
b. 00000111
c. 00001111
d. 10001000
22. The advantage with normalized floating-point number is
a. easy to represent
b. any base number can be represented
c. provide maximum possible precision
d. requires less number of CPU registers
23. A floating point number is said to be normalized
a. if the most significant digit of the mantissa is nonzero
b. if the most significant digit of the mantissa is zero
c. if mantissa is positive
d. if exponent is positive
24. In floating point representation the radix
a. must be represented physically
b. is assumed and not represented physically
c. has no significance
d. is represented separately along with position of radix point
25. In floating point representation the radix position
a. must be represented physically
b. is assumed and not represented physically
c. has no significance
d. is represented separately along with position of radix point
26. A normalized floating-point decimal number is
a. 0.03456
b. 3.456
c. 34.56

d. 3456

27. The two parts in floating-point representation are
a. radix, mantissa
b. mantissa, base
c. mantissa , exponent
d. radix, exponent
28. The part in floating-point representation that denotes position of the radix point is
a. exponent
b. mantissa
c. base
d. both exponent and mantissa
29. In floating point representation, the fixed point mantissa
a. must be integer
b. may be integer
c. must be fraction
d. may be fraction or integer
30. In floating point representation, the fixed point mantissa
a. must be positive
b. may be positive
c. is signed number
d. must be negative
31. A normalized floating-point binary number is
a. 0.01010
b. 1010
c. 10.10
d. 1.010
32. Odd parity generator can be implemented with
a. AND function
b. OR function
c. exclusive & OR function
d. Exclusive - OR & Exclusive - Nor function
33. If 3 bit messages are transmitted suffixing with P (odd) bit the erroneous message is
a. 1011
b. 0111
c. 0010
d. 1010
34. Parity checker networks are constructed with logic circuits comprising
a. AND logic gates
b. OR logic gates
c. exclusive OR logic gates
d. NOR logic gates
35. Even parity generators can be implemented with
a. AND functions
b. OR functions
c. exclusive OR functions
d. NOR functions
36. If 3 bit messages are transmitted suffixing with P (even) bit the erroneous message is
a. 0110
b. 1100
c. 0100

d. 1111
37. If a 3 bit message 010 is transmitted with suffix of even parity bit , the resultant Message is
a. 0100
b. 0101
c. 1010
d. 0010
38. If a 3 bit message 101 is transmitted with suffix of even parity bit , the resultant Message is
a. 1010
b. 1011
c. 0101
d. 1101
39. If a 3 bit message 110 is transmitted with suffix of odd parity bit , the resultant Message is
a. 1100
b. 1101
c. 0110
d. 1110
40. If a 3 bit message 011 is transmitted with suffix of odd parity bit , the resultant Message is
a. 0011
b. 1011
c. 0110
d. 0111
41. Even parity generator is constructed with logic circuits comprising
a. AND logic gates
b. OR logic gates
c. exclusive OR logic gates
d. NOR logic gates
42. A Common bus system is connected with four registers of 4-bit capacity using binary MUXs . The number of MUXs required is
a. 4
b. 8
c. 3
d. 16
43. A Common bus system is connected with four registers of 4-bit capacity using binary MUXs. The size of each MUX each is
a. 8 X 1
b. 4 X 1
c. 16 X 1
d. 12 X 1
44. The function that allows register transfer under a predetermined condition is
a. **Conditional variable**
b. Sample function
c. Control function
d. RTL function
45. The state of the three-state gate when input is not connected to output is
a. 0

b. 1
c. forbidden
d. high impedence state
46. Register transfer denoting memory write operation is
a. **DA ←M {[AR]}**
b. **M {[AR]}←DR**
c. **M←DR**
d. **DR←M**
47. The operation executed on data stored in registers is called
a. RTL instruction
b. Micro operation
c. Register logic
d. Nano operation
48. The symbolic notation used to describe the micro operation transfers among registers is
called
a. **Register Transfer language**
b. Micro operations
c. Nano operation
d. Assembly language
49. The symbolic form used to denote transfer of content of register R1 into register R2 is
a. R2=R1
b. R1 >R2
c. **R1 ← R2**
d.
50. **The arithmetic micro operation R3←R1+ +1 denotes**
a. The sum of R1 and R2 transferred to R3
b. The sum of 1's complement of R1 and R2
c. The sum of 2's complement of R1 and R2
d. **Subtraction of R2 from R1**
51. The arithmetic micro operation denoting negation is
a. **R3←R1+R2**
b. **R3←R1+R2**
c. **R2← +1**
d. **R1←R1+1**
52. **The arithmetic micro operation R2← +1 denotes**
a. The sum of R1 and R2 transferred to R3
b. 1's complement of R2
c. 2's complement of R2
d. Increment of R2
53. The arithmetic micro operation denoting subtraction of R3 from R1 is
a. **R3←R1+R2**
b. **R1←R1+ +1**
c. **R2← +1**
d. **R3← +R3+1**
AA
54. **The arithmetic micro operation denoting 2's complement is**
a. **R1←R1+1**

b. **R1←R1-1**
c. **R1← +1**
d. **R1←**
55. **The arithmetic micro operation denotes**
a. The sum of R1 and R2 is transferred to R3
b. The difference of R1 and R2 is transferred to R3
c. Complements the content of R2
d. Increment the content of R1 by one
56. **On executing the arithmetic micro operation R2←**
a. The sum of R1 and R2 is transferred to R3
b. The difference of R1 and R2 is transferred to R3
c. Content of R2 is Complemented
d. Content of R1 is incremented by one
57. **The arithmetic micro operation denoting decrementing the content of R1 by one is**
a. **R1←R1+1**
b. **R1←R1-1**
c. **R1← +1**
d. **R1←**
58. **The arithmetic micro operation denoting 1's complement is**
a. **R1←R1+1**
b. **R1←R1-1**
c. **R1← +1**
d. **R1←**
59. **The arithmetic micro operation denoting complement is**
a. **R1←R1+1**
b. **R1←R1-1**
c. **R1← +1**
d. **R1←**
60. **The logic micro operation used to selectively set bits is**
a. **F←**
b. **F←B⊕ A**
c. **F←A - B**
d. **F←B ∩B**
61. The logic micro operation used to selectively clear bits is
a. **F←**
b. **F←B∪A**
c. **F←A⊕ B**
d. **F←A ∩B**
62. The logic Micro operation that denotes clear is
a. **F←A ∩ B**
b. **F←A-B**
c. **F←A**
d. **F←0**
63. The logic micro operation that denotes AND is
a. **F←A ∩ B**
b. **F←**

c. **F←A- B**
d. **F**
64. The logic micro operation that denotes transfer A is
a. **F←**
b. **F←A∩A**
c. **F←A-A**
d. **F←A**
65. **The logic micro operation that denotes exclusive NOR is**
a. F-A,B
b. **F←A∩B**
c. **F←A-B**
d. **F**
66. The logic micro operation that denotes complement of B is
a. **F←**
b. **F←B∩A**
c. **F←B-B**
d. **F←B∩B**
67. The category of micro operation used for serial transfer of data is
a. Arithmetic micro operation
b. logical micro operation
c. shift micro operation
d. Register Transfer micro operation.
68. **The function denoted by arithmetic operation F=A+ is**
a. Subtraction
b. subtraction with borrow
c. 2's complement
d. 1's complement
69. The shift micro operation used to multiply signed binary number by 2 is
a. Shift left
b. Circuit shift left
c. Arithmetic shift left
d. Arithmetic shift right
70. The shift micro operation used to divide signed binary number by 2 is
a. Shift left
b. Circuit shift left
c. Arithmetic shift left
d. Arithmetic shift right
71. The function denoted by arithmetic operation F=A+B+1 is
a. Addition
b. 2s complement
c. Add with carry
d. increment
72. **If the content of 8 bit register R1 is 11010011 . The content of register R1 after execution**
of R1←shr R1 micro operation is
a. 01101001
b. 11101001
c. 10100110

d. 10100111

73. **If the content of 8 bit register R1 is 11010011. The content of register R1 after execution of R1←shl R1 micro operation is**

a. 01101001
b. 11101001
c. 10100110
d. 10100111

74. **If the content of 8 bit register R1 is 10001101. The content of register R1 after Execution of R1←Cir R1 micro operation is**

a. 11000110
b. 00011011
c. 01000110
d. 00011010

75. **If the content of 8 bit register R1 is 11010011. The content of register R1 after execution of R1 ← ashr R1 micro operation is**

a. 01101001
b. 10100110
c. 10100111
d. 11101001

76. The function denoted by arithmetic operation F=A-1 is

a. 1's complement
b. **subtraction with borrow**
c. 2's complement
d. decrement

77. The general-purpose computer register is

a. Data Register
b. Accumulator
c. Instruction register
d. Program counter

78. In direct addressing mode address part of instruction specifies

a. Address of next instruction
b. Address of register
c. Address of operand in memory
d. Operand itself

79. The computer register used to hold address of instruction is

a. Data Register
b. Accumulator
c. Instruction register
d. Program counter

80. The computer register that specifies memory address is

a. Address register
b. Accumulator
c. Instruction register
d. Temporary register

81. If it takes 5ns to read an instruction from memory, 2ns to decode the instruction, 3ns

To read the register file, 4ns to perform the computation required by the instruction, and 2ns to write the result into the register file, what is the maximum clock rate of the processor?
a. 62.5 MHz
b. 20 MHz
c. 25 MHz
d. 6.25 MHz
82. The part of instruction code that specifies operation to be performed is
a. opcode
b. address
c. binary operand
d. the complete Instruction code
83. In IAS computer address part specifies
a. Address of next instruction
b. Address of register
c. Address of operand in memory
d. Operand itself
84. In indirect addressing mode address part of instruction specifies
a. Address of next instruction
b. Address of current instruction
c. Address of operand
d. Address of memory location containing address of operand
85. The computer register used to hold instruction code is
a. Data Register
b. Accumulator
c. Instruction register
d. Program counter
86. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. Draw the instruction word format and indicate the number of bits in each.
a. indirect 1bit, Opcode 5bits, Register 8bits, Address 18 bits
b. indirect 1bit, Opcode 15its, Register 8bits, Address 8 bits
c. indirect 1bit, Opcode 8bits, Register 8bits, Address 15 bits
d. indirect 1bit, Opcode 7bits, Register 9bits, Address 15 bits
87. The instruction that clears start stop flip flop and stops sequence counter from counting
is
a. CLA
b. INC
c. SNE
d. HLT
88. A computer uses a instruction format that has three parts: an indirect part, and operationcode, and an address part. One of the operand is AC and is implicit. Another operand isspecified in the address part. An instruction at 021 has I=0, an operation code of the ANDinstruction, and an address part equal to 083 (all numbers are in hexadecimal) containsthe operand B8 F2 and the content of AC is A937. Go over the instruction cycle anddetermine the contents of the following registers at the end of the execute phase: PC, AR,DR, AC, and IR.
a. 022, 083, B8F2, A832, 021

b. 021, 021, B8F2, A937, 021
c. 022, 022, A937, A832, 022
d. 021, 022, A937, B8F2,.021
89. Which of the following statement(s) is(are) correct?
a. CISC has more complex circuitry than RISC
b. CISC architectures tend to take more space in memory than the same programs written for RISC architecture.
c. RISC architecture have more addressing modes than the CISC architecture.
d. RISC has more complex circuitry than RISC
90. Match the following:
1. Immediate i.) Multiple memory references
2. Direct ii.) No memory reference
3. Indirect iii.) One memory reference
a. 1:iii, 2:ii, 3:i
b. 1:ii, 2:iii, 3:i
c. 1:i, 2:ii, 3:iii
d. 1:ii, 2:i, 3:iii
91. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer.
a. 4
b. 8
c. 16
d. 32
92. In the instruction cycle the phase that reads instruction into instruction register from memory is
a. Fetch
b. Decode
c. Read effective address
d. execute the instruction
93. In the instruction cycle the phase that reads effective address from memory location is
a. Fetch
b. Decode
c. Read effective address
d. execute the instruction
94. The instruction that increments accumulator is
a. CLA
b. INC
c. SNE
d. HLT
95. The instruction that clears accumulator is
a. CLA
b. INC
c. SNE
d. HLT
96. **The memory reference instruction that denotes operation M[AR]←M[AR]+1, if M[AR]+1=0 then PC←PC+1 is**
a. AND

b. BSA
c. BUN
d. ISZ

97. **The memory reference instruction that denotes operation M[AR]←PC,PC ←AR+1 is**
a. AND
b. BSA
c. BUN
d. ISZ

98. **The memory reference instruction that denotes operation PC ←AR is**
a. AND
b. BSA
c. BUN
d. STA

99. **The input-output instruction that denotes operation If (FGI =1) then PC←PC+1 is**
a. INP
b. SKI
c. SKO
d. ION

100.**The Input-Output Instruction that denotes operation If (FGO =1) then PC←PC+1 is**
a. INP
b. SKI
c. SKO
d. ION

101.**The memory reference instruction that denotes operation AC ← AC ∩ M[AR] is**
a. AND
b. ADD
c. LDA
d. STA

102.**The memory reference instruction that denotes operation M[AR]←AC is**
a. AND
b. BSA
c. BUN
d. STA

103.**The memory reference instruction that denotes operation AC ← M[AR] is**
a. AND
b. BSA
c. BUN
d. LDA

104.**In the process of information transfer to input register from input device the initial Value of control flip-flop FGI is**
a. 0(Zero)
b. 1 (one)
c. 2 (two)
d. 8 (eight)

105.In the process of information transfer to output register from accumulator the initial value of control flip-flop FGO is
a. 0(Zero)
b. 1 (one)

c. 2 (two)
d. 8 (eight)
106.The CPU organization in which all operations are performed with an implied Accumulator register is
a. General register Organization
b. Stack organization
c. Shared memory organization
d. Single accumulator organization
107.The CPU organization that does not use an address field for the instructions is
a. General register Organization
b. Stack organization
c. Shared memory organization
d. Single accumulator organization
108.The CPU organization in which all operations are performed with two or three Register fields is
a. General register organization
b. Stack organization
c. Shared memory organization
d. Single accumulator organization
109.In Register Stack the stack pointer register (SP) contains
a. The word that is currently on top of stack
b. The address of the word that is currently on top of stack
c. The highest address of stack
d. The lowest address of stack
110.The addressing mode in which the address part of the instruction is added to Program counter in order to obtain effective address is
a. Direct Address mode
b. Register Mode
c. Relative Address Mode
d. Register Indirect Mode
111.The DATA transfer instruction is
a. MOV
b. DEC
c. NEG
d. SUB B
112.The addressing mode in which the address part of the instruction gives effective Address of operand is
a. Direct Address mode
b. Register Mode
c. Indirect Addressing Mode
d. Register Indirect Mode
113.The addressing mode in which the address part of the instruction gives address of effective address of operand is
a. Direct Address mode
b. Register Mode
c. Indirect Address Mode
d. Register Indirect Mode
114.The DATA manipulation instruction is
a. MUL

b. LD
c. MOV
d. PUSH
115.The addressing mode that specifies operands implicitly in the definition of the Instruction is
a. Immediate Mode
b. Register Mode
c. Implied Mode
d. Register Indirect Mode
116.The addressing mode that specifies operand in the instruction itself is
a. Immediate Mode
b. Register Mode
c. Implied Mode
d. Register Indirect Mode
117.The addressing mode that specifies register operands is
a. Direct Address mode
b. Register Mode
c. Implied Mode
d. Register Indirect Mode
118.The addressing mode that specifies register containing address of operands is
a. Direct Address mode
b. Register Mode
c. Implied Mode
d. Register Indirect Mode
119.The shift instruction is
a. ROR
b. IN
c. NEG
d. DEC
120.The program control instruction that do not change program sequence directly is
a. BR
b. RET
c. SKP
d. CMP
121.The status bit that is set to 1 if the exclusive-OR of the last two carries is equal to 1 is
a. C (Carry)
b. S (sign)
c. Z (zero)
d. V (Overflow)
122.The program control instruction that sets the status bits by performing logical AND of the two operands is
a. BR
b. RET
c. SKP
d. TST
123.The program control instruction that sets the status bits by performing a subtraction between two operands is
a. CMP
b. RET

c. SKP
d. TST
124.The interrupts that arise from illegal or erroneous use of an instruction or data are
a. External interrupts
b. Internal interrupts
c. Subroutine Calls
d. Software interrupts
125.The program control instruction that is used in conjunction with subroutines is
a. BR
b. RET
c. SKP
d. TST
126.The program control instruction that does not need an address field is
a. BR
b. RET
c. SKP
d. TST
127.The characteristic that is not applicable for RISC architecture is
a. Fixed Length instruction format
b. Memory access is limited to load and store instructions
c. Micro program control
d. All operations within registers of CPU
128.The characteristic that is not applicable for CISC architecture is
a. Fixed Length instruction format
b. A large variety of addressing modes
c. Some specialized instructions
d. Instructions that manipulate operands in memory
129.Internal interrupts are also called as
a. Signals
b. Traps
c. System Calls
d. Subroutine Calls
130.The most computers based on RISC architecture concept use
a. Address generator
b. program counter
c. Instruction register
d. Sub routine register
131.The alternate way of implementing mapping function instead of ROM is
a. Programmed Logic Array
b. using RAM
c. Using Microprocessor
d. using Micro controller
132.The next address generator in a micro programmed control unit is referred to as
a. Address generator
b. Sequencer
c. Instruction register
d. Program counter
133.The process of transferring instruction code bits to an address in control memory Where the routine is located is referred as

a. address translation
b. Micro program execution
c. Mapping
d. address generation
134.The address of next microinstruction is stored in
a. Control address Register (CAR)
b. Sub routine register (SBR)
c. Instruction register (IR)
d. Program counter (PC)
135.The function of control unit in digital computer is
a. to generate micro operations
b. to update micro operations
c. to initiate sequence of micro operations
d. to add new micro operations
136.If the control signals are generated using hardware with conventional logic design techniques then the control unit is said to be
a. Micro programmed
b. Hardwired
c. Nano programmed
d. Programmed
137.The memory that is part of control unit is
a. Main memory
b. Auxiliary memory
c. Control memory
d. Virtual memory
138.Micro instructions are stored in
a. Main memory
b. Secondary memory
c. Control memory
d. Virtual memory
139.The register used to store return address of sub routine is
a. Control address Register (CAR)
b. Sub routine register (SBR)
c. Instruction register (IR)
d. Program counter (PC)
140.The Pseudo-instruction that specifies first address of a micro program routine is
a. ORG
b. PCTAR
c. DRTAR
d. CALL
141.The symbolic microinstructions that loads SBR with a new value is
a. JMP
b. CALL
c. RET
d. MAP
142.Most computers based on RISC architecture
a. use micro programmed control unit
b. use hardwired control unit
c. use nano programmed control unit

d. does not require control unit
143.The program that translates symbolic micro program into its binary equivalent is
a. Compiler
b. Assembler
c. Interpreter
d. Parser
144.A system uses a control memory of 1024 words of 32bits each. The microinstruction has
three fields: Condition, Branch address, and Microperation fields. If the microoperation field has 16 bits, how many bits are there in the branch address field and the condition field?
a. Branch address has 10 bits and condition field has 6 bits
b. Branch address has 6 bits and condition field has10 bits
c. Branch address has 8 bits and condition field has 8 bits
d. Branch address has 9 bits and condition field has 7 bits
145.Assume that the control memory is 24 bits wide. The microinstruction has two fields: Address and Microoperation fields. If the microoperation has 13 bits, how many bits are there in the address field and what is the size of the control memory?
a. Address field has 11 bits and the size of the control memory is 2048x24 bits.
b. Address field has 10 bits and the size of the control memory is 1024x24bits.
c. Address field has 11 bits and the size of the control memory is 1024x24bits.
d. Address has 24 bits and the size of the control memory is 2048x24bits.
146.Arrange the following with the increasing speed of execution.
a. Horizontal microinstruction, vertical microinstruction, hardwired implementation
b. Vertical microinstruction, horizontal microinstruction, hardwired implementation.
c. Hardwired implementation, vertical microinstruction, horizontal mincroinstruction.
d. Hardwired implementation, horizontal microinstruction, vertical microinstruction.
147.Arrange the following with the increasing logic of circuitry.
a. Horizontal microinstruction, vertical microinstruction, hardwired implementation
b. Vertical microinstruction, horizontal microinstruction, hardwired implementation.
c. Hardwired implementation, vertical microinstruction, horizontal Microinstruction.
d. Hardwired implementation, horizontal microinstruction, vertical microinstruction.
148.Which of the following statement(s) is(are) correct ?
a. The horizontal microinstruction requires more bits than vertical microinstruction.
b. Changes can be easily accommodated in hardwired control unit than in micro programmed
control unit.
c. Hardwired control unit is cheaper than microprogrammed control unit.
d. Vertical microinstruction canbe executed fascal than horizantal microinstruction
149.Which of the following statement(s) is(are) correct?
a. Variable microinstruction format increases complexity of microprogram control unit.
b. Horizontal micro programmed control unit requires additional circuitry for decoding.
c. Concurrency is fully exploited in vertical microprogrammed control unit than in horizantal
microprogrammed control unit.
d. Variable micro instruction format decreases complexity of microprogram control

unit.
150.Match the following:
1. microoperation i. Operations executed on data stored in registers
2. microinstruction ii. Sequence of microinstructions
3. microprogram iii. Sequence of microoperations
a. 1:i, 2:iii, 3:ii
b. 1:i, 2:ii, 3:iii
c. 1:ii, 2:i, 3:iii
d. 1:ii, 2:iii, 3:i
151.In performing addition and subtraction of signed 2's complement data, if an overflow occurs
a. there will an erroneous results in AC
b. AC contains no erroneous result
c. AC becomes zero
d. Content of accumulator has no significance
152.In adding two signed magnitude numbers, parallel adder is implemented with
a. half adders
b. full adders
c. decodes
d. encoders
153.Let A(0111) and B(1001) be two BCD numbers. The sum of A and B in BCD is
a. 0000 with a carry of 1
b. 0110 with a carry of 1
c. 0110 with a carry of 0
d. 0000 with a carry of 1
154.BCD adder performs sum in binary and converts the binary sum to valid BCD representation whenever the binary sum is greater than 1001. Invalid binary sum is corrected by
a. adding binary 6 (0110) to the binary sum
b. adding binary 9 (1001) to the binary sum
c. subtracting binary 6 (0110) to the binary sum
d. subtracting binary 9 (1001) to the binary sum
155.The 9`s complement of a BCD number is obtained by complementing the bits in the coded representation with a correction. The correction is
a. binary 10 (1010) is added to each complemented digit and the carry is discarded after each addition
b. binary 6 (0110) is added before the digit is complemented
c. binary 10 (1010) is added before the digit is complemented
d. binary 6 (0110) is added to each complemented digit and the carry is discarded
156.**What will be the quotient and remainder when is divided by in 2's complement binary representation?**
a. Quotient 00000; Remainder 10101
b. Quotient 00000; Remainder 01011
c. Quotient 10101: Remainder 00000
d. Quotient 01011; Remainder 00000
157.**What will be the quotient and remainder when is divided by in 2's complement representation?**
a. Quotient 00000; Remainder 01011
b. Quotient 00000; Remainder 10101

c. Quotient 00000; Remainder 00000
d. Quotien 01011; Remainder 00000
158.The 9's complement of BCD number 0111 is
a. 1000
b. 1001
c. 0010
d. 0011
159.Consider register A holding decimal 8760 in BCD. The micro operation dshr A (Decimal shift right register A) produces.
a. 1000 0111 0111 0000
b. 0100 0011 1011 0000
c. 1100 0011 1011 0000
d. 0000 1000 0111 0110
160.Consider register A holding decimal 8760 in BCD. The micro operation dshl A (Decimal shift left register A) produces.
a. 1000 0111 0110 0000
b. 0000 1110 1100 0000
c. 0111 0110 0000 1000
d. 0111 0110 0000 0000
161.**The signed magnitude representation of in BCD is**
a. 1001 0010 0111 0101
b. 1111 0010 0111 0101
c. 0001 0010 0111 0101
d. 0000 0010 0111 0101
162.**The 9's complement representation of in BCD is**
a. 1001 0111 0010 0100
b. 1111 0111 0010 0100
c. 0001 0111 0010 0100
d. 0001 1101 1000 1010
163.**The 10's complement representation of in BCD is**
a. 1001 0111 0010 0101
b. 1111 0111 0010 0101
c. 0001 1000 0011 0110
d. 0001 1101 1000 1011
164.**Express the number in IEEE 32-bit floating-point format**
a. 0 1000 0111 1000 0000 0000 0000 0000 000
b. 0 0000 1000 1000 0000 0000 0000 0000 000
c. 0 0000 1000 1100 0000 0000 0000 0000 000
d. 0 1000 0111 1100 0000 0000 0000 0000 000
165.Express the number -1/32 in IEEE 32-bit floating point format
a. 1 0111 1010 0000 0000 0000 0000 0000 000
b. 1 0000 0001 0000 0000 0000 0000 0000 000
c. 1 0000 0001 1000 0000 0000 0000 0000 000
d. 1 0111 1010 1000 0000 0000 0000 0000 000
166.**Use IEEE single-precision floating-point numbers to compute the (32) X(16) .**
a. 0 0000 0111 0000 0000 0000 0000 0000 000
b. 0 1000 1000 0000 0000 0000 0000 0000 000
c. 0 0111 0111 0000 0000 0000 0000 0000 000

d. 0 1000 1000 1000 0000 0000 0000 0000 000
167.**Use IEEE single-precision floating-point number to compute (32) ÷ (16) .**
a. 0 0000 0000 1000 0000 0000 0000 0000 000
b. 0 0000 0001 0000 0000 0000 0000 0000 000
c. 0 1000 0000 0000 0000 0000 0000 0000 000
d. 0 1000 0000 1000 0000 0000 0000 0000 000
168.**Use IEEE single-precision floating-point numbers to compute (147.5) +(0.25) .**
a. 0 1000 0110 0010 0111 1000 0000 0000 000
b. 0 1000 0110 0010 0111 0000 0000 0000 000
c. 0 0111 1101 0010 0111 1000 0000 0000 000
d. 0 0111 1101 0010 0111 0000 0000 0000 000
169.To perform multiplication of two signed 2's complemented numbers using Booths algorithm, when the multiplier bit is identical to the previous multiplier bit
a. The multiplicand is subtracted from partial product
b. The multiplicand is added to the partial product
c. The multiplicand is multiplied with partial product
d. The partial product does not change
170.Which of the following statement(s) is(are) correct?
a. No overflow can occur in the addition operation of binary numberts
b. Division operation may never result in a quotient with an overflow in binary division
c. An overflow can be detected in addition whenever the carry into the sign bit position and the carry out of the sign bit position are not equal in binary addition
d. Over flow can occur in the multiplication operation of binary numbers
171.Which of the following statement(s) is(are) in correct?
a. A divide overflow condition occurs if the high-order bits of the dividend constitute a number
greater than or equal to the divisor
b. Multiplication of two n-digit numbers in base r gives a product no more than 2n digits in length
c. An overflow canbe defected in addition whenever the carry into the sign bit position and the
carry out of the sign bit position are not equal in binary addition.
d. Binary division operation may never result in a quotient overflow.
172.Which of the following statement(s) is(are) correct?
a. Booth's algorithm treats both positive and negative 2's complement n-bit operands uniformly
b. Booth's algorithm treats both positive and negative 2's complement n-bit operands uniformly
&There can be no mantissa overflow after a multiplication operation in floating point representation
c. There can be no mantissa overflow after a multiplication operation in floating point representation
d. Booth's algorithm is for unsigned multiplication only
173.**What is the sum of in BCD?**
a. 0000 0001 1000
b. 0000 1100 1000

c. 0000 0010 1000
d. 0001 0001 1000
174.In performing floating-point addition, or subtractions , if two exponents are not equal then
a. mantissa having larger exponent is shifted to the left
b. mantissa having larger exponent is shifted to the right
c. mantissa having smaller exponent is shifted to the left
d. mantissa having smaller exponent is shifted to the right
175.What value is represented by the following IEEE single precision floating-point number
1 0111 1010 1000 0000 0000 0000 0000 0000 000
a. -84
b. -0.03125
c. -.0.046875
d. -0.46875
176.**BCD adder performs sum in binary and converts the binary sum to valid BCD representation whenever the binary sum is greater than 1001. Let the binary sum be labeled as where K is the carry are labels of four bits in binary sum in that order. The condition for a correction can be expressed by the Boolean function.**
a.
b.
c.
d.
177.**BCD adder performs sum in binary and converts the binary sum to valid BCD representation whenever the binary sum is greater than 1001. Let the binary sum be labeled as where K is the carry are labels of four bits in binary sum in that order. The condition for an output carry can be expressed by the Boolean function.**
a.
b.
c.
d.
178.Multiplication of two floating point numbers requires
a. Addition of mantissas and multiplication of exponents
b. Addition of exponents and multiplication of mantissas
c. Multiplication mantissas only
d. Addition of exponents only
179.Division of two floating point numbers requires
a. Subtraction of mantises and division of exponents
b. Subtraction of exponents and division of mantissas
c. Subtraction of exponents only
d. Division of mantissas only
180.**What is the signed binary product of in binary?**
a. 1101110001
b. 0010001111
c. 0100010001
d. 1000010001
181.Which of the following statement(s) is(are) correct?
a. For a fixed format, a larger exponent base gives a greater range of expressible values at the expense of less precision.

b. For a fixed format, a larger exponent base gives a greater range of expressible values and good precision.
c. For a fixed format, a larger exponent base gives good precision but lesser range of expressible values.
d. Precision or range of expressible numbers does not depend on exponent.
182.In floating point arithmetic operation, for each arithmetic operation
a. the results will be normalized
b. the results will not be normalized
c. the results will be in BCD
d. the result will be in 2s complement form
183.In decimal multiplication the sequence counter (SC) is set to
a. number of bits in multiplier
b. number digits in multiplier
c. number of bits in multiplicand
d. number digits in multiplicand
184.In Decimal Arithmetic operations decimal number are stored in
a. 1s complement form
b. 2s compliment form
c. BCD form
d. Signed magnitude form
185.Decimal arithmetic operations use
a. Half adders
b. Full adders
c. BCD adders
d. Parallel adders
186.**In decimal arithmetic the symbolic designation A←A+B represents**
a. add decimal numbers A and B and transfer sum into A
b. add decimal numbers A and B and transfer sum into A in binary
c. add binary numbers A and B and transfer sum into A as decimal number
d. **add binary numbers A and B and transfer sum into A in binary**
187.**In decimal arithmetic the symbolic designation represents**
a. 1's complement of B
b. 2's complement of B
c. 10's complement of B
d. 9's complement of B
188.**In decimal arithmetic the symbolic designation +1 represents**
a. 1's complement of B
b. 2's complement of B
c. 10's complement of B
d. 9's complement of B
189.In decimal arithmetic the symbolic designation dshr A represents
a. binary shift right register A
b. decimal shift right register A
c. binary left register A
d. decimal shift left register A
190.In decimal arithmetic the symbolic designation dshl A represents
a. binary shift right register A

b. decimal shift right register A
c. binary left register A
d. decimal shift left register A