JNTU ONLINE EXAMINATIONS [Mid 2 - co]

1. "Locality of Reference" is related to: [01D01]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

2. Expand CAM [01D02]
a. Cache Access Memory
b. Call Access Mode
c. Contents Addressable Memory
d. Cache Access Module

3. Associative Memory is like [01D03]
a. Primary Memory
b. Secondary Memory
c. Cache Memory
d. Auxiliary Mem ory

4. In the Memory Hierarchy, top to bottom (Registers to Tape) [01M01]
a. Capacity Decreases
b. Capacity Increases
c. Speed Increases
d. Cost per bit Increases

5. In the Memory Hierarchy, top to bottom (Registers to Tape) [01M02]
a. Cost per bit decreases
b. Cost per bit Increases
c. Speed Increases
d. Access Time Decreases

6. In the Memory Hierarchy, bottom to top (Tape to Registers) [01M03]
a. Speed Decreases
b. Access time Increases
c. Capacity Increa ses
d. Capacity Decreases

7. In the Memory Hierarchy, top to bottom (Registers to tape) [01M04]
a. Speed Increases
b. Speed decreases
c. Cost per bit Increases
d. Access time decreases

8. In the Memory Hierarchy, the following Memory has least capacity [01S01]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

9. In the Memory Hierarchy, the following Memory has maximum Access time [01S02]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

10. In the Memory Hierarchy, the following Memory has least Access time [01S03]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

11. In the Memory Hierarchy, Speed of accessing is high for [01S04]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

12. In the Memory Hierarchy, Speed of accessing is low for [01S05]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

13. In the following which is accesed sequentially [01S06]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

14. In the Memory Hierarchy, Cost per bit is least for [01S07]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

15. In the Memory Hierarchy, the Cost per bit is most for [01S08]
a. Register
b. Cache
c. Primary Memory
d. Magnetic Tape

16. 512 x 8 ROM indicates [02D01]
a. 512 data, 8 address lines
b. 512 address, 8 data lines
c. 520 address lines
d. 520 data lines

17. The Static RAM consis ts of [02M01]
a. Capacitors
b. Internal Flip Flops
c. Internal Caches
d. Filters

18. The Dynamic RAM consists of [02M02]
a. Capacitors
b. Internal Flip Flops
c. Internal Caches
d. Filters

19. The decoder used for decoding 512 x 8 ROM consists of how many input lines? [02S01]
a. 512
b. 8
c. 9
d. 520

20. The Principal technology used for main Memory is based on [02S02]
a. Semi conductor ICs
b. Conductor ICs
c. Both Semi Conductor and Conductor ICs
d. Using Insulator

21. Refreshing is required for [02S03]
a. All RAMs
b. Only DRAMs
c. Only SRAMs
d. Both SRAMs and DRAMs

22. Boot Strap loader requires [02S04]
a. RAM
b. ROM
c. Any Memory
d. Only Processor

23. By making programs and data available at a rapid rate, it is possible to [03D01]
a. Decrease the performance
b. Increase the performance

c. Save Memory
d. Reduce cost

24. The part of the computer system that supervises the flow of information between Auxiliary Memory and Main Memory is called [03D02]
a. Processor Management System
b. Data Management System
c. Address Management System
d. Memory Management System

25. Existence of two or more programs in different parts of the Memory Hierarchy at the same time is defined as: [03M01]
a. Uni programming
b. Multi programming
c. Multi processing
d. Uni processing

26. If Cache Acces s time is 100ns, Memory access time is 1000ns, if the hit percentage is 100 %, what is the Average access time [03M02]
a. 100
b. 1000
c. 1100
d. 10

27. If both Cache Memory and Main Memory are updated for a write operation, the type of the Cache Memory is called [03M03]
a. Write-back
b. Write-through
c. Associative
d. TLB

28. If only Cache location is updated during a Write operation as long as there is no replacement, the type of the Cache Memory is called [03M04]
a. Write-back
b. Write-through
c. Associative
d. TLB

29. Replacing the block that has been not used for the longest period of time is [03M05]
a. FIFO
b. LRU
c. MRU
d. LFU

30. Replacing the page that entered the Memory at first is [03M06]
a. FIFO
b. LRU
c. MRU
d. LFU

31. A faster and smaller Memory in between CPU and main Memory is [03S01]
a. Primary Memory
b. Secondary Memory
c. Cache Memory
d. Auxiliary Mem ory

32. To compensate speed mismatch between main Memory and Processor, the Memory used is [03S02]
a. Primary Memory
b. Secondary Memory
c. Cache Memory
d. Auxiliary Mem ory

33. If Hit ratio is 0.8, the miss ratio [03S03]
a. 9.2
b. 92 %
c. 0.2
d. 20 %

34. In the following, which is not a Cache Mapping technique [03S04]
a. Associative Mapping
b. Direct Mapping
c. Test-Associative Mapping
d. Set-Associative Mapping

35. In four-way Set-Associative mapping, the number of tags are [03S05]
a. One
b. Two
c. Four
d. Sixteen

36. In the following, which is the fastest mapping technique [03S06]
a. Direct Mapping
b. Associative Mapping
c. Test-Associative Mapping
d. Set-Associative Mapping

37. In Cache, the data stored is [03S07]
a. Most frequently used
b. Least frequently used
c. Never used
d. Segment with large data

38. The transfer of data between main Memory and Cache is [03S08]
a. WORD
b. BLOCK
c. LINE
d. CHARACTER

39. The transfer of data between Processor and Cache is [03S09]
a. WORD
b. BLOCK
c. FRAME
d. CHARACTER

40. "Beladys Anomaly" does not occur in [04D01]
a. FIFO
b. LRU
c. MRU
d. Optimal replacement

41. In Paging technique, the logical address space is [04M01]
a. Divided into equal parts
b. Divided into unequal parts
c. divided into two parts
d. Either equal or unequal parts

42. The technique of Segmentation suffers which fragmentation [04M02]
a. Internal
b. External
c. both Internal and External
d. Neither Internal nor External

43. "Paged Segmentation" has [04M03]
a. Internal fragmentation
b. External fragmentation
c. Zero fragmentation
d. Neither Internal nor Externa l

44. The time taken to access a particular track is [04S01]
a. Seek time
b. Latency time
c. Access time
d. Burst time

45. The time taken to access a particular sector is [04S02]
a. Seek time
b. Latency time

c. Access time
d. Burst time

46. For a magnetic tape, the access is [04S03]
a. Random Access
b. Sequential Access
c. Both Random and Sequential
d. Rotational

47. For a magnetic disc, the access is [04S04]
a. Direct Acc ess
b. Sequential Access
c. Both Random and Sequential
d. Rotational

48. The technique of Paging suffers which fragmentation [04S05]
a. Internal
b. External
c. both Internal and External
d. Neither Internal nor External

49. By using TLB in Paged segmentation [05D01]
a. Access time decreases
b. Access time increases
c. Speed decreases
d. Fragmentation decreases

50. Contents addressable Memory (CAM) is related to [05D02]
a. Page table
b. Associative Page table
c. Inverted Page table
d. Normal Page table

51. If there are sixteen bits in the Virtual Address format, the size of the Virtual Address is [05M01]
a. 16K words
b. 16 words
c. 64 K words
d. 16M words

52. If the size of the Page is 1K for a Virtual Address space of 16K, the size of the Frame in main Memory is [05M02]
a. 16K
b. 8K
c. 4K
d. 1 K

53. Discs that are permanently attached to the unit assembly and cannot be removed by the occasional user are called [05S01]
a. Floppy discs
b. Hard discs
c. External discs
d. Flash Memory

54. A disk drive with a removable disk is [05S02]
a. Hard disk
b. Floppy disk
c. Permanent disk
d. Cache

55. In the following, which is not a P hysical Memory [05S03]
a. Primary Memory
b. Cache Memo ry
c. Flash Memory
d. Virtual Memory

56. Which Page Replacement technique is most efficient [05S04]
a. FIFO
b. LRU
c. MRU

d. LFU

57. Page table contains [05S05]

a. Starting address of Page
b. Page no., Frame no.
c. Length of the page
d. Page no., Segme nt no.

58. Number of P rinting Characters in ACSII code are [06D01]

a. 128
b. 94
c. 34
d. 8

59. Number of Non Printing Characters in ACSII code are [06D02]

a. 128
b. 94
c. 34
d. 8

60. ASCII code uses how many bits [06M01]

a. 5
b. 7
c. 8
d. 9

61. The Cathode Ray Tube contains an electronic gun which can be deflected [06M02]

a. Only horizontally
b. Only vertically
c. Both horizontally and vertically
d. Neither horizontally nor vertically

62. Input/Output devic es connec ted to the computer are also called as [06S01]

a. Modems
b. Routers
c. Peripherals
d. Processors

63. Which of the following is not a P rinter? [06S02]

a. Inkjet printer
b. Dot Matrix
c. Laser Printer
d. Scanner

64. In the following which is sequentially accessed [06S03]

a. Magnetic Disc
b. Magnetic Tape
c. Flash Memory
d. Cache Memo ry

65. The command used to activate the peripheral and to inform it what to do is [07D01]

a. Control command
b. Status com mand
c. Data output com mand
d. Data input com mand

66. The command that causes the interface to respond by transferring data from the Bus into one of its registers is [07D02]

a. Control command
b. Status com mand
c. Data output command
d. Data input com mand

67. The command used that causes the interface to receive an item of data from the peripheral and places it in its Buffer register is [07D03]

a. Control command
b. Status com mand
c. Data output com mand
d. Data input command

68. In Asynchronous data transfer, both sender and receiver accompany a control signal that is: [07M01]

a. Strobe
b. Hand Shaking
c. Two wire control
d. Single wire control

69. The circuit which provides the interface between computer and similar interactive terminal is [07M02]

a. USRP
b. UART
c. Flip Flop
d. D-Flip Flop

70. The command used to test various status conditions in the interface and the peripheral is [07S01]

a. Control command
b. Status command
c. Data output com mand
d. Data input com mand

71. In the following which mapping does not distinguish Memory address and I/O address [07S02]

a. Memory mapped I/O
b. Isolated I/O
c. Independent I/O
d. Interrupt driven I/O

72. In the following which mapping uses different address space for Memory and I/O [07S03]

a. Memory mapped I/O
b. Isolated I/O
c. Independent I/O
d. Interrupt driven I/O

73. The rate at which Serial information is transmitted and is equivalent to the data transfer in bits per second is [07S04]

a. Baud rate
b. Bit rate
c. Control rate
d. Strobe rate

74. In Daisy chaining, the number of interrupt request lines is (are) [08D01]

a. n
b. 2n
c. only one
d. changes

75. In Daisy chaining, the number of interrupt acknowledge lines is (are) [08D02]

a. n
b. 2n
c. only one
d. changes

76. In the following, which is not priority interrupt method [08D03]

a. Polling
b. Daisy chaining
c. Parallel priority
d. Direct Memory Access

77. In the following, which is efficient [08M01]

a. Programmed I/O
b. Interrupt initiated I/O
c. Direct Memory Access
d. All the equally eff icient

78. In the following, which uses separate controller for data transfer [08M02]

a. Programmed I/O
b. Interrupt initiated I/O
c. Direct Memory Access
d. Memory mapped I/O

79. In Polling, the drawback is [08M03]
a. Cost is more
b. Complex hardware is required
c. Time consuming
d. Maintenance is more

80. Daisy Chaining is [08M04]
a. Software me thod
b. Hardware method
c. Both software and hardware
d. Neither software nor hardware

81. In the following, which is not a mode of transfer [08S01]
a. Programmed I/O
b. Interrupt initiated I/O
c. Direct Memory Access
d. Memory mapped I/O

82. In Priority interrupt when two devices interrupt the computer at the same, the computer services the device [08S02]
a. with larger length at first
b. with shorter length at first
c. with highest priority at first
d. with lowest priority at first

83. In Daisy chaining, device with highest priority is in [08S03]
a. First position
b. Middle position
c. Last position
d. Any position

84. Continuously monitoring I/O devices is done in [08S04]
a. Programmed I/O
b. Interrupt initiated I/O
c. Direct Memory Access
d. Memory mapped I/O

85. In the following, which is more time consuming [08S05]
a. Programmed I/O
b. Interrupt initiated I/O
c. Direct Memory Access
d. Memory mapped I/O

86. A block sequence consisting of a number of Memory words is transferred continuously while a DMA controller is master of Memory Bus. This is [09D01]
a. Polling
b. Daisy Chaining
c. Burst transfer
d. Cycle Stealing

87. DMA controller transfer one data word at a time and transfers the control of the Bus to CPU. This is [09M01]
a. Polling
b. Daisy Chaining
c. Burst transfer
d. Cycle Stealing

88. In the following, which is a method related to DMA. [09S01]
a. Polling
b. Daisy Chaining
c. Parallel Priority
d. Cycle Stealing

89. For fast transfer of information between Magnetic Disc and Memory, which of the following is recommended [09S02]
a. Programmed I/O
b. Daisy Chaining
c. Polling

d. DMA

90. The DMA controller acts like [09S03]

a. Primary Memory

b. CPU

c. Cache Memo ry

d. Router

91. The number of basic I/O commands in IBM 370 computer IOP is [10D01]

a. 50

b. 6

c. 8

d. 40

92. The number of basic I/O commands in Intel 8089 computer IOP is [10D02]

a. 50

b. 6

c. 8

d. 40

93. The Intel 8089 I/O processor contains the IC package of [10M01]

a. 64 pins

b. 40 pins

c. 16 pins

d. 32 pins

94. A Processor with Direct Memory Access capability that communicates with I/O devices is [10S01]

a. Input Output Processor

b. Data comm unication processor

c. Data comm unication programmer

d. Input Output programmer

95. A process or that communicates with remote terminals over telephone and other communication media in a serial fashion is called [10S02]

a. Input Output Processor

b. Data communication processor

c. Data comm unication programmer

d. Input Output programmer

96. The I/O processor in IBM 370 computer is called [10S03]

a. Router

b. Channel

c. Device

d. Modem

97. Let the time taken to process a sub-operation in each segment be 20ns. Assume That the pipeline has 4 segments and executes 100 tasks in sequence. What is the Speed up of pipeline system? [11D01]

a. 8000ns

b. 3060ns

c. 2060ns

d. 6000ns

98. The _ _ _ _ _ _ _ _ _ _ _ architecture represents the organization of a computer containing a single control unit, a processor unit and a memory unit. [11M01]

a. SIMD

b. MISD

c. SISD

d. MIMD

99. Total operations performed going through all the segments in the pipeline is called as _ _ _ _ _ _ _ _ [11M02]

a. function

b. process

c. sequence

d. task

100. One type of parallel processing that does not fit Flynn s classification is _ _ _ _ _ _ _ _ processing. [11M03]

a. array
b. vector
c. multi
d. pipeline

101. The sequence of instructions read from memory constitutes _ _ _ _ _ _ _ _ [11S01]
a. data stream
b. execution stream
c. instruction stream
d. process stream

102. Most of the multi processors and multi computer systems can be classified in _ _ _ _ _ _ _ _ category. [11S02]
a. MISD
b. SIMD
c. SISD
d. MIMD

103. The behavior of a pipeline can be illustrated with _ _ _ _ _ _ _ diagram [11S03]
a. frequency-time
b. timing
c. space-time
d. dataflow

104. As the number of tasks increases, the speed up is equal to the number of _ _ _ _ _ _ in the pipeline [11S04]
a. tasks
b. segments
c. suboperations
d. instructions.

105. Suppose the time delays of four segments are $t_1 = 60ns, t_2 = 70ns, t_3 = 100ns, t_4 = 80ns$ **and the interface registers have a delay of** t_r**=10ns. What must be the clock cycle time? [12D01]**
a. 100ns
b. 120ns
c. 110ns
d. 130ns

106. Each entry in the BTB consists of the address of a previously executed _ _ _ _ _ _ _ _ instruction and the _ _ _ _ _ _ _ _ instruction for that branch [12D02]
a. branch, target
b. branch, buffer
c. target, branch
d. buffer, branch

107. _ _ _ _ _ _ _ _ _ conflicts arise when an instruction depends on the result of a previous instruction [12M01]
a. resource
b. branch
c. segment
d. data dependency

108. When an overflow occurs, the mantissa of the sum or difference is shifted _ _ _ _ _ _ And exponent incremented by _ _ _ _ _ _ [12M02]
a. right, one
b. left, one
c. right, two
d. left, two

109. A _ _ _ _ _ _ _ pipeline divides an arithmetic operation into suboperations for execution in the pipeline segments. [12S01]
a. vector
b. arithmetic
c. instruction
d. multiple

110. _ _ _ _ _ _ _ _ pipeline operates on a stream of instructions by overlapping phases of instruction cycle. [12S02]

a. arithmetic
b. instruction
c. vector
d. multiple

111. The instruction fetch segment can be implemented by means of a _ _ _ _ _ _ buffer [12S03]
a. LIFO
b. FIFO
c. FILO
d. LILO

112. The instruction stream queuing mechanism provides an efficient way for reducing _ _ _ _ _ _ _ _ _ _ for reading instructions from memory [12S04]
a. access time
b. seek time
c. overlapping time
d. processing time

113. _ _ _ _ _ _ _ _ _ is a circuit that detects instructions whose source operands are destinations of instructions further up in the pipeline [12S05]
a. operand forwarding
b. interlocks
c. delayed load
d. data decoder

114. The method used in mos t RISC processors is to rely on the compiler to redefine the branches so that they take effect at the proper time in the pipeline. This method is called _ _ _ _ _ _ _ _ _ _ [13D01]
a. delayed branch
b. delayed load
c. delayed store
d. delayed add

115. The RISC consists of only _ _ _ _ _ _ _ _ length instruction format [13M01]
a. variable
b. fixed
c. small number
d. large number

116. The data transfer instructions in RISC are limited to _ _ _ _ _ _ _ and _ _ _ _ _ _ _ _ instructions [13M02]
a. add, sub
b. mul, div
c. load, store
d. in, out

117. Since all operands are in registers, there is no need for _ _ _ _ _ _ _ _ of operands from memory [13S01]
a. fetch
b. decode
c. execute
d. store

118. The concept of delaying the use of the data loaded from memory is referred to as _ _ _ _ _ _ _ _ _ _ [13S02]
a. delayed branch
b. delayed load
c. delayed store
d. delayed add

119. The compiler for a proc essor that uses delayed branches is designed to analyze the instructions _ _ _ _ _ _ _ _ _ _ the branch [13S03]
a. before
b. after
c. before & after
d. later

120. A computer capable of vector processing eliminates the overhead associated with the time it

takes to _ _ _ _ _ _ _ _ and _ _ _ _ _ _ _ _ _ _ the instructions in the program loop [14D01]

a. fetch, decode
b. fetch, execute
c. execute, decode
d. fetch, store

121. A vector processor that uses an n-way interleaved memory can fetch _ _ _ _ _ _ _ _ _ _ operands from _ _ _ _ _ _ _ _ _ different modules [14D02]

a. n, n
b. n, m
c. 1, 1
d. 1, 2

122. Matrix _ _ _ _ _ _ _ is one of the most computational intensive operations performed In computers with vector processors [14M01]

a. addition
b. subtraction
c. transpose
d. multiplication

123. A computer with vector instructions and pipelined floating-point arithmetic operations is referred to as _ _ _ _ _ _ _ _ computer [14M02]

a. mini
b. ma infram e
c. super
d. micro

124. A measure used to evaluate computers in their ability to performs a given number of floating-point operations per second is referred as _ _ _ _ _ _ _ _ _ _ [14M03]

a. MIPS
b. KIPS
c. FLOPS
d. BAUDS

125. _ _ _ _ _ _ _ _ _ _ processing deals with computations involving large matrices [14S01]

a. arithmetic
b. parallel
c. pipeline
d. vector

126. Aerodynamics and space flight simulations uses _ _ _ _ _ _ _ _ _ _ processing [14S02]

a. vector
b. arithmetic
c. parallel
d. pipeline

127. In _ _ _ _ _ _ _ memory, different sets of addresses are assigned to different memory modules [14S03]

a. associate
b. random
c. interleaved
d. multiple

128. A vector is an ordered set of _ _ _ _ _ _ _ _ _ dimensional array of data items [14S04]

a. two
b. three
c. one
d. four

129. Instruction format for vector instruction is _ _ _ _ _ _ _ _ address instruction [14S05]

a. zero
b. one
c. two
d. three

130. One of the following _ _ _ _ _ _ _ _ _ system is an example for array processor [15D01]

a. VAX
b. PDP-11

c. MPP
d. ILLIAC- IV

131. Each processing element of SIMD will have _ _ _ _ _ _ _ _ _ _ memory [15D02]
a. global
b. shared
c. local
d. temporary

132. An array processor consists of _ _ _ _ _ _ _ _ _ _ instructions and _ _ _ _ _ _ _ data organization [15M01]
a. single, multiple
b. multiple, single
c. single, single
d. multiple, multiple

133. The objective of the attached array processors is to provide _ _ _ _ _ _ _ _ capabilities to a conventional computer [15M02]
a. high speed
b. pipelined
c. parallel
d. vector manipulation

134. The function of the master control unit in SIMD processor is to _ _ _ _ _ _ _ _ _ _ _ _ the instruction [15M03]
a. fetch
b. decode
c. execute
d. store

135. _ _ _ _ _ _ _ _ _ _ _ array processor is an auxiliary processor attached to a general purpose computer [15S01]
a. attached
b. auxiliary
c. parallel
d. distributed

136. The attached processor is a _ _ _ _ _ _ _ _ machine driven by the host computer [15S02]
a. front-end
b. back-end
c. ma ster
d. slave

137. Scalar and program controlled instructions are directly executed with in the _ _ _ _ _ _ _ unit [15S03]
a. master control
b. me mory
c. PE
d. local memory

138. The system with the attached processor satisfies the needs for _ _ _ _ _ _ _ _ arithmetic applications [15S04]
a. complex
b. simple
c. scalar
d. vector

139. _ _ _ _ _ _ _ _ _ _ _ schemes are used to control the status of each PE during the execution [15S05]
a. masking
b. blocking
c. delayed
d. translation

140. The inter process communication mechanism used in loosely coupled system is _ _ _ _ [16D01]
a. pipes
b. FIFO
c. shared m em ory

d. message queues

141. Tightly c oupled systems can tolerate a _ _ _ _ _ _ _ degree of interaction between tasks [16D02]

a. no
b. higher
c. lower
d. minimal

142. Multiprocessing can improve performance by decomposing a program into _ _ _ _ _ _ _ executable tasks [16M01]

a. serial
b. parallel
c. multiple
d. several

143. _ _ _ _ _ _ _ _ technology has reduced the cost of computer components very much. [16M02]

a. SSI
b. MSI
c. VLSI
d. LSI

144. Multiprocessors are classified as multiple processor _ _ _ _ _ _ _ _ systems [16S01]

a. SISD
b. MIMD
c. SIMD
d. MISD

145. _ _ _ _ _ _ _ _ _ architecture forms a computer network [16S02]

a. multiprocessor
b. multi computer
c. single computer
d. distributed computer

146. Each processor element in a _ _ _ _ _ _ _ _ _ system has its own private local memory [16S03]

a. tightly coupled
b. loosely coupled
c. time shared
d. multistage

147. The inter process communication mechanism used in tightly coupled system is _ _ _ _ [16S04]

a. pipes
b. FIFO
c. shared memory
d. me ssage queues

148. The _ _ _ _ _ _ _ _ _ _ interconnection is suitable for connecting small number of processors [17D01]

a. cross bar
b. multiport
c. multi stage
d. hypercube

149. The basic component of a multi stage network is a 2 -input 2-output interchange _ _ _ _ _ [17D02]

a. crossbar
b. connection point
c. switch
d. hub

150. _ _ _ _ _ _ _ _ _ memory system employees separate buses between each memory module and each CPU [17M01]

a. common bus
b. multiport
c. crossbar
d. multistage switch

151. A three cube structure consists of _ _ _ _ _ _ _ nodes [17M02]

a. 1
b. 2

c. 4
d. 8

152. _ _ _ _ _ _ _ _ _ _ consists of a number of points that are placed at intersections between processor buses and memory parts [17S01]
a. cross bar
b. multiport
c. common bus
d. hypercube

153. _ _ _ _ _ _ _ _ _ _ is used to control the communication between a number of sources and destinations [17S02]
a. cross bar
b. multiport
c. commonbus
d. multistage switch

154. The _ _ _ _ _ _ _ _ multiprocessor struc ture is a loosely coupled system with 2n processors [17S03]
a. crossbar
b. multi port
c. hypercube
d. multistage switch

155. A single common bus system is restricted to transfer _ _ _ _ _ _ _ _ _ _ processor at a time [17S04]
a. one
b. two
c. ma ny
d. IOP

156. _ _ _ _ _ _ _ _ multiprocessor system consists of a number of processors connected through a common path to a memory unit [17S05]
a. common bus
b. multiport
c. crossbar
d. hypercube

157. The crossbar switch consists of _ _ _ _ _ _ _ _ _ _ _ _ devices [17S06]
a. decoder
b. encoder
c. multiplexer
d. de-multiplexer

158. The IEEE 796 standard bus has _ _ _ _ _ _ _ _ data _ _ _ _ _ _ _ address and _ _ _ _ _ _ _ _ control lines [18D01]
a. 36,24,36
b. 10,24,30
c. 16,24,26
d. 16,20,20

159. _ _ _ _ _ _ _ _ _ _ _ _ must be performed to resolve multiple contention for the shared resources [18D02]
a. arbitration
b. multiplexing
c. looping
d. controlling

160. The processor in a shared memory multiprocessor system request access to common memory through _ _ _ _ _ _ _ _ _ [18M01]
a. system bus
b. internal bus
c. synchronized bus
d. asynchronus bus

161. The parallel bus arbitration technique uses _ _ _ _ _ _ _ _ priority encoders and decoders [18M02]
a. internal

b. ma ximum
c. external
d. low

162. The _ _ _ _ _ _ _ _ _ _ _ _ _ _ algorithm gives the highest priority to the reques ting device that has not used the bus for the longest interval [18M03]
a. polling
b. LRU
c. FIFO
d. time slice

163. In _ _ _ _ _ _ _ _ bus , each data item is transferred during a time slice known to source and destination in advance [18S01]
a. serial
b. parallel
c. synchronus
d. asynchronus

164. In serial arbitration procedure the device closest to the priority line is assigned _ _ _ _ _ _ _ priority [18S02]
a. low
b. high
c. normal
d. no

165. The _ _ _ _ _ _ _ _ algorithm allocates a fixed length time slice of bus time to each processor [18S03]
a. polling
b. LRU
c. FIFO
d. time slice

166. In the _ _ _ _ _ _ _ _ _ _ scheme , requests are served in the order received [18S04]
a. polling
b. LRU
c. FIFO
d. time slice

167. The _ _ _ _ _ _ _ _ _ _ _ sequence is normally programmable and as a result the selection priority can be altered under program control [18S05]
a. polling
b. LRU
c. FIFO
d. time slice

168. Out of the following which one is the hardware instruction to implement semaphore [19D01]
a. flag
b. turn
c. spin
d. test and set

169. To protect data from being changed simultaneously by 2 or more processors is called _ _ _ _ _ _ _ _ _ _ [19M01]
a. protection
b. access matrix
c. hiding
d. mutual exclusion

170. _ _ _ _ _ _ _ _ _ _ _ _ _ is often used to indicate whether or not a processor is exec uting a critical section [19M02]
a. mo nitor
b. spin lock
c. semaphore
d. rendezbous

171. _ _ _ _ _ _ _ _ _ is the common communication mechanism used between processors [19S01]
a. FIFO
b. semaphore

c. shared memory
d. me ssage queue

172. _ _ _ _ _ _ _ _ _ _ _ multiprocessor system memory is distributed among the processors and there is no shared memory for passing information [19S02]
a. tightly coupled
b. shared mem ory
c. loosely coupled
d. specialized

173. A _ _ _ _ _ _ _ _ _ _ _ _ is a program sequence that once begun must complete execution before another processor access the same shared resource [19S03]
a. critical section
b. entry section
c. mutual exclusion
d. exit section

174. A scheme that allows writable data to exist in atleast one cache is a method that employees _ _ _ _ _ _ _ _ _ in its compiler [20D01]
a. distributed local table
b. distributed global table
c. centralized local table
d. centralized global table

175. A memory scheme is _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ if the value returned on a load instruction is always the value given by the latest store instruction with the same address [20M01]
a. conflict
b. coherence
c. concurrent
d. coupling

176. The bus controller that monitors the cache coherence problem is referred as _ _ _ _ _ _ _ [20M02]
a. snoopy cache controller
b. split cache controller
c. direct cache controller
d. side cache controller

177. In _ _ _ _ _ _ _ _ mechanism both cache and main memory are updated with every write operation [20S01]
a. write back
b. write both
c. write through
d. write once

178. In _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ mechanism only the cache is updated and the location is marked so that it can be copied later into main memory [20S02]
a. write back
b. write both
c. write through
d. write once