Code No: R09220501 **R09** **Set No. 2**

II B.Tech II Semester Examinations,Dec/Jan 2011
COMPUTER ORGANIZATION
Common to Chemical Engineering, Computer Science And Engineering
Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate I/O Bus and memory Bus.
   (b) What are major functional differences between memory mapped I/O and Isolated I/O. [7+8]
2. (a) Explain RISC pipeline in detail.
   (b) Explain vector processing. [7+8]
3. Design a circuit which can be used to transfer data from any register to any other register out of four 4-bit registers A,B,C,D which uses RS flip-flops. [15]
4. (a) Explain the functioning of a control unit explaining the terms control word, control memory, control address register and control buffer register.
   (b) Support the statement. Instruction Set Architecture has impact on the processors microarchitecture. [7+8]
5. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [5+5+5]
6. (a) Explain the terms NaN, overflow and underflow in the IEEE 754 representation of floating point numbers.
   (b) Explain 2's complement method of representing numbers. When can you say that an overflow has occurred when adding or subtracting two fixed point numbers.
   (c) What do you mean by a parity bit? Explain with an example how even and odd parity bits are generated. Is it possible to correct errors using parity bits. [5+5+5]
7. (a) Draw a circuit for 10's complement of a given numbers.
   (b) Explain the relative advantages and disadvantages of 9's and 10's complement methods. [7+8]
8. (a) What are the total number of switches in a 8×8 omega network? Show a neat sketch.
   (b) How many nodes will be there in a 4 Dimensional hyper cube? Show a neat sketch. [7+8]

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Code No: R09220501 **R09** **Set No. 4**

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1. (a) What are the relative advantages of ones complement and two's complement methods.
   (b) Explain subtraction procedure using complement representation. [7+8]
2. (a) What is Flynn's classification? Categorize the different streams in it.
   (b) Explain SIMD array processor prganization. [7+8]
3. (a) What are the different interconnection structures used in multiprocessors? Explain about multistage crossbar switch.
   (b) Support or oppose the statement? Every efficient serial program is efficient parallel program? [7+8]
4. (a) What are the different types of I/O communication techniques? Give brief notes.
   (b) In the above techniques, which is the most efficient? Justify your answer.[7+8]
5. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processors instruction set, simply write a C program and compile and store the resultant code in control memory.
   (b) Why do we need subroutine register in a control unit? Explain. [7+8]
6. (a) Explain the functioning of omega switching network with a neat sketch.
   (b) In 8 × 8 omega switching network how many stages are there and in each stage how many Switches are there.
   (c) How many stages and how many Switches in each stage are needed in a n × n omega sitching network. [5+5+5]
7. (a) Differentiate between paging and segmentation.
   (b) What are the relative advantages and disadvantages of using the technique of paged segmentation.
   (c) In the Paged Segmentation technique, if the logical address format is as shown in the diagram below

Segment No.	Page No.	Offset
2 bits	4 bits	10 bits

   i. What is the maximum size of virtual memory required?
   ii. What is the maximum size of one segment?
   iii. What is the size of each page?

iv. How many maximum number of pages are possible for each segment? [15]

8. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [15]

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1. (a) Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also, draw a circuit using full adders for the same.
   (b) Explain Booth's logorithm with its theoretical basis. [7+8]
2. Describe commonly employed bit shift operators such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D Flip-Flops. [15]
3. (a) What is a virtual memory technique? Explain different virtual memory techniques.
   (b) Explain how the technique of paging can be implemented. [7+8]
4. (a) What is meant by arithmetic pipeline? Explain.
   (b) Explain pipeline for floating point addition and subtraction. [7+8]
5. (a) Explain how Flynn classified the processors into different streams by giving an example for each stream.
   (b) Explain tightly coupled and loosely coupled systems with suitable examples. [7+8]
6. (a) Give the typical horizontal and vertical microinstruction formats.
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [7+8]
7. What are relative advantages and disadvantages of I/O communication techniques? Explain. [15]
8. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity? What is odd function and even function? To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [15]

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Code No: R09220501 **R09** **Set No. 3**

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Answer any FIVE Questions
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1. (a) What is Flynn's classification? Categorize.
   (b) Explain each stream of the Flynn's classification with an example. [5+10]
2. What are various components involved in serial communication? Explain. [15]
3. Perform the following arithmetic operations using 2's complement method and 1's complement method.
   (a) 1101−011
   (b) 1111−1001
   (c) 1111−1111
   (d) 0111−1101. [4+4+3+4]
4. (a) Explain how the Bit Cells are organized in a Memory Chip.
   (b) Explain the organization of a 1K × 1 Memory with a neat sketch. [7+8]
5. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows.
   (b) Explain the term 'memory bus bottleneck'.
   (c) Distinguish between multiprocessor and a multicomputer. [5+5+5]
6. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [7+8]
7. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors. [5+5+5]
8. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction is completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [15]

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