Code No: 07A5EC01   **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., I Mid-Term Examinations, September – 2010
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. ☐☐☐☐☐ A ☐☐☐☐

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I   **Choose the correct alternative:**

1. _____ is concerned with the way the hardware components connected together to form the computer system   [   ]
   a) Computer Architecture   b) Computer Design
   c) Computer Monitoring   d) Computer Organization

2. $(xy)^1$ states _____ according to Demorgan's Law   [   ]
   a) $x^1 y^1$ b) $(xy)^1$ c) $(x^1 + y^1)$ d) Insufficient data

3. Convert $(41.6875)_{10}$ to _____ binary   [   ]
   a) $(101001.1011)_2$ b) $(10100.11011)_2$
   c) $(1010011.011)_2$ d) $(10100110.11)_2$

4. A bus system can be constructed with a high impedance state is   [   ]
   a) Resistant state   b) Capacitance State
   c) High Impedance State   d) Process State

5. Booths multiplication algorithm specifies a procedure for multiplying two Binary integers in [   ]
   a)signed 2's compliment   b) signed 1's compliment
   c) signed magnitude   d) none of the above

6. To design a common bus system for 4 register of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder?   [   ]
   a) 2 to 4 Decoder   b) 3 to 8 Decoder   c) 4 to 16 Decoder   d)5 to 32 decoder

7. If the address field of an instruction specifies the effective address, then the instruction is [   ]
   a) Immediate Instruction   b) Direct Instruction
   c) Indirect Instruction   d) None

8. When two normalized mantissas are added, the sum may contain   [   ]
   a) Underflow   b) Overflow   c) no Underflow   d) no Overflow

9. The advantage of biased exponent is that the exponent is represented as   [   ]
   a) Positive Number   b) Negative Member   c) Unsigned Number   d) None

10. Which of the following is also called the next address generator for a Control memory   [   ]
    a) Multiplier   b) Micro program sequencer
    c) Control Address Register   d) Program Counter

II   Fill in the blanks:

11.   _____ is a group of bits that instruct the computer to perform a specific operation.

12.   _____ holds the address of the instruction to be fetched from the memory.

13.   Fetching the instruction from memory is called as _____

14.   The concurrent execution of several application programs to make the best possible use of computer resources by the operating system known as _____

15.   After the arithmetic shift left operation of a register, if there is sign reversal, then _____ occurs.

16.   The type of shift used to shift the contents of a register which contains a signed binary number is called _____

17.   In a memory stack, after the pop operation, the stack pointer will be _____

18.   Immediate corresponds to _____ reference instructions.

19.   BSA corresponds to _____ type instruction.

20.   If the memory size is 4096*16, then _____ address lines are required to address any memory location

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Code No: 07A5EC01   **Set No. 2**

Name: _____ Hall Ticket No. ☐☐☐☐☐ A ☐☐☐☐

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I   Choose the correct alternative:

1.   A bus system can be constructed with a high impedance state is   [   ]
      a) Resistant state   b) Capacitance State
      c) High Impedance State   d) Process State

2.   Booths multiplication algorithm specifies a procedure for multiplying two Binary integers in [   ]
      a)signed 2's compliment   b) signed 1's compliment
      c) signed magnitude   d) none of the above

3.   To design a common bus system for 4 register of 4-bits each, by using tristate buffers and a
      decoder, what is the size of the decoder?   [   ]
      a) 2 to 4 Decoder   b) 3 to 8 Decoder   c) 4 to 16 Decoder   d)5 to 32 decoder

4.   If the address field of an instruction specifies the effective address, then the instruction is [   ]
      a) Immediate Instruction   b) Direct Instruction
      c) Indirect Instruction   d) None

5.   When two normalized mantissas are added, the sum may contain   [   ]
      a) Underflow   b) Overflow   c) no Underflow   d) no Overflow

6.   The advantage of biased exponent is that the exponent is represented as   [   ]
      a) Positive Number   b) Negative Member   c) Unsigned Number   d) None

7.   Which of the following is also called the next address generator for a Control memory   [   ]
      a) Multiplier   b) Micro program sequencer
      c) Control Address Register   d) Program Counter

8.   _____ is concerned with the way the hardware components connected together to form the
      computer system   [   ]
      a) Computer Architecture   b) Computer Design
      c) Computer Monitoring   d) Computer Organization

9. $(xy)^1$ states _____ according to Demorgan's Law   [   ]
      a) x^1y^1 b) $(xy)^1$ c) (x^1+y^1) d) Insufficient data

10.   Convert $(41.6875)_{10}$ to _____ binary   [   ]
      a) $(101001.1011)_2$ b) $(10100.11011)_2$
      c) $(1010011.011)_2$ d) $(10100110.11)_2$

II Fill in the blanks:

11. The concurrent execution of several application programs to make the best possible use of computer resources by the operating system known as _____

12. After the arithmetic shift left operation of a register, if there is sign reversal, then _____ occurs.

13. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

14. In a memory stack, after the pop operation, the stack pointer will be _____

15. Immediate corresponds to _____ reference instructions.

16. BSA corresponds to _____ type instruction.

17. If the memory size is 4096*16, then _____ address lines are required to address any memory location

18. _____ is a group of bits that instruct the computer to perform a specific operation.

19. _____ holds the address of the instruction to be fetched from the memory.

20. Fetching the instruction from memory is called as _____

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Code No: 07A5EC01   **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., I Mid-Term Examinations, September – 2010
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. [ ][ ][ ][ ][ ][A][ ][ ][ ][ ]

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I   Choose the correct alternative:

1.   To design a common bus system for 4 register of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder?   [   ]
        a) 2 to 4 Decoder   b) 3 to 8 Decoder   c) 4 to 16 Decoder   d)5 to 32 decoder

2.   If the address field of an instruction specifies the effective address, then the instruction is [   ]
        a) Immediate Instruction   b) Direct Instruction
        c) Indirect Instruction   d) None

3.   When two normalized mantissas are added, the sum may contain   [   ]
        a) Underflow   b) Overflow   c) no Underflow   d) no Overflow

4.   The advantage of biased exponent is that the exponent is represented as   [   ]
        a) Positive Number   b) Negative Member   c) Unsigned Number   d) None

5.   Which of the following is also called the next address generator for a Control memory   [   ]
        a) Multiplier   b) Micro program sequencer
        c) Control Address Register   d) Program Counter

6.   _____ is concerned with the way the hardware components connected together to form the computer system   [   ]
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        c) Computer Monitoring   d) Computer Organization

7. $(xy)^1$ states _____ according to Demorgan's Law   [   ]
        a) x^1y^1 b) $(xy)^1$ c) (x^1+y^1) d) Insufficient data

8.   Convert $(41.6875)_{10}$ to _____ binary   [   ]
        a) $(101001.1011)_2$ b) $(10100.11011)_2$
        c) $(1010011.011)_2$ d) $(10100110.11)_2$

9.   A bus system can be constructed with a high impedance state is   [   ]
        a) Resistant state   b) Capacitance State
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10.   Booths multiplication algorithm specifies a procedure for multiplying two Binary integers in [   ]
        a)signed 2's compliment   b) signed 1's compliment
        c) signed magnitude   d) none of the above

II Fill in the blanks:

11. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

12. In a memory stack, after the pop operation, the stack pointer will be _____

13. Immediate corresponds to _____ reference instructions.

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17. _____ holds the address of the instruction to be fetched from the memory.

18. Fetching the instruction from memory is called as _____

19. The concurrent execution of several application programs to make the best possible use of computer resources by the operating system known as _____

20. After the arithmetic shift left operation of a register, if there is sign reversal, then _____ occurs.

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   a) x^1y^1 b) $(xy)^1$ c) (x^1+y^1) d) Insufficient data

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20.   In a memory stack, after the pop operation, the stack pointer will be _____

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