**Code No: 07A5EC01** **Set No. 1**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**III B.Tech I-Sem I Mid-Term Examinations, September– 2009**

**COMPUTER SYSTEM ORGANIZATION**

**Objective Exam**

**Name: _____ Hall Ticket No.** | | | | | | A | | | | |

**Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.**

## I Choose the correct alternative:

1. The range of numbers that can be represented by *n* – bit register, if the numbers are represented in 2's complement format. [ ]
   a) $-(2^{n-1} - 1)$ to $+ (2^{n-1} - 1)$ b) $-(2^{n-1})$ to $+(2^{n-1} - 1)$
   c) $-(2^{n-1} - 1)$ to $+(2^{n-1})$ d) $-(2^{n-1})$ to $+ (2^{n-1})$

2. In a typical instruction format, the type of operation to be performed is specified by [ ]
   a) Mode field b) opcode field c) Address field d) None

3. The number of different logic operations that can be performed with '*n*' – binary variables is [ ]
   a) $2^n$ b) $2^{n+1}$ c) $2^{n-1}$ d) $2^{2^n}$

4. In which of the data transfer scheme, the computer monitors continuously the input and output flags, before performing data transfer? [ ]
   a) Interrupt initiated transfer b) Program controlled transfer
   c) DMA transfer d) None

5. Booth's multiplication algorithm specifies a procedure for multiplying two binary integers in . [ ]
   a) Signed 2's complement b) Signed 1's complement
   c) Signed magnitude d) None of the above

6. To design a common bus system for 4 registers of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder? [ ]
   a) 2 to 4 Decoder b) 3 to 8 Decoder c) 4 to 16 Decoder d) 5 to 32 Decoder

7. If the address field of an instruction specifies the address of a memory location where effective address is available the instruction is [ ]
   a) Immediate Instruction b) Direct Instruction
   c) Indirect Instruction d) None of the above

8. The range of numbers that can be represented by *n*- bit integer, if the numbers are represented in signed magnitude format. [ ]
   a) $\pm (2^{n-1} - 1)$ b) $\pm (2^{n-1})$ c) $+ (2^{n-1})$ to $- (2^{n-1}-1)$ d) $- (2^{n-1}-1)$ to $+ (2^{n-1})$

9. To design a common bus system for 4 registers of 16-bits each, what is the size of each multiplexer? [ ]
   a) 2 x 1 MUX b) 4 x 1 MUX c) 8 x 1 MUX d) 16 x 1 MUX

**Cont...2**

**Code No: 07A5EC01** **Set No. 1**

10. The instruction code consists of one mode bit, three Opcode bits and 12 address bits. For an input – output instruction the combination of mode bit and Opcode bits will be [ ]
a) 0111 b) 1111 c) 0110 d) 1110

## II. Fill in the blanks:

11. In a Array multiplier circuit with 'j' multiplier bits and 'k' multiplicand bits, the number of AND gates required are _____

12. In a memory stack, before every push operation, the stack pointer wll be _____

13. A divide overflow condition occurs, if the high order half bits of the dividend is _____

14. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

15. Arithmetic expressions can be evaluated more effectively by using _____Organization.

## III. Match the following:

| | | | |
|---|---|---|---|
| 16. | Autodecrement Mode | [ ] | a) Input output instructions |
| 17. | Data Register | [ ] | b) Memory reference instructions |
| 18. | Instruction Register | [ ] | c) Loops |
| 19. | S K I | [ ] | d) Holds the instruction code |
| 20. | I S Z | [ ] | e) Holds the data brought from memory |

**-oOo-**

**Code No: 07A5EC01** **Set No. 2**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**III B.Tech I-Sem I Mid-Term Examinations, September– 2009**

**COMPUTER SYSTEM ORGANIZATION**

**Objective Exam**

**Name: _____ Hall Ticket No.** | | | | | | A | | | | |

**Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.**

## I Choose the correct alternative:

1. In which of the data transfer scheme, the computer monitors continuously the input and output flags, before performing data transfer? [ ]
   a) Interrupt initiated transfer b) Program controlled transfer
   c) DMA transfer d) None

2. Booth's multiplication algorithm specifies a procedure for multiplying two binary integers in . [ ]
   a) Signed 2's complement b) Signed 1's complement
   c) Signed magnitude d) None of the above

3. To design a common bus system for 4 registers of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder? [ ]
   a) 2 to 4 Decoder b) 3 to 8 Decoder c) 4 to 16 Decoder d) 5 to 32 Decoder

4. If the address field of an instruction specifies the address of a memory location where effective address is available the instruction is [ ]
   a) Immediate Instruction b) Direct Instruction
   c) Indirect Instruction d) None of the above

5. The range of numbers that can be represented by *n*- bit integer, if the numbers are represented in signed magnitude format. [ ]
   a) $\pm (2^{n-1} - 1)$ b) $\pm (2^{n-1})$ c) $+ (2^{n-1})$ to $- (2^{n-1}-1)$ d) $- (2^{n-1}-1)$ to $+ (2^{n-1})$

6. To design a common bus system for 4 registers of 16-bits each, what is the size of each multiplexer? [ ]
   a) 2 x 1 MUX b) 4 x 1 MUX c) 8 x 1 MUX d) 16 x 1 MUX

7. The instruction code consists of one mode bit, three Opcode bits and 12 address bits. For an input – output instruction the combination of mode bit and Opcode bits will be [ ]
   a) 0111 b) 1111 c) 0110 d) 1110

8. The range of numbers that can be represented by *n* – bit register, if the numbers are represented in 2's complement format. [ ]
   a) $-(2^{n-1} - 1)$ to $+ (2^{n-1} - 1)$ b) $-(2^{n-1})$ to $+(2^{n-1} - 1)$
   c) $-(2^{n-1} - 1)$ to $+(2^{n-1})$ d) $-(2^{n-1})$ to $+ (2^{n-1})$

9. In a typical instruction format, the type of operation to be performed is specified by [ ]
   a) Mode field b) opcode field c) Address field d) None

**Cont...2**

**Code No: 07A5EC01** **Set No. 2**

10. The number of different logic operations that can be performed with '*n*' – binary variables is [ ]

a) $2^n$ b) $2^{n+1}$ c) $2^{n-1}$ d) $2^{2^n}$

## II. Fill in the blanks:

11. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

12. Arithmetic expressions can be evaluated more effectively by using _____Organization.

13. In a Array multiplier circuit with 'j' multiplier bits and 'k' multiplicand bits, the number of AND gates required are _____

14. In a memory stack, before every push operation, the stack pointer wll be _____

15. A divide overflow condition occurs, if the high order half bits of the dividend is _____

## III. Match the following:

| | | | | |
|---|---|---|---|---|
| 16. | Autodecrement Mode | [ | ] | a) Input output instructions |
| 17. | Data Register | [ | ] | b) Memory reference instructions |
| 18. | Instruction Register | [ | ] | c) Loops |
| 19. | S K I | [ | ] | d) Holds the instruction code |
| 20. | I S Z | [ | ] | e) Holds the data brought from memory |

**-oOo-**

**Code No: 07A5EC01** **Set No. 3**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**III B.Tech I-Sem I Mid-Term Examinations, September– 2009**

**COMPUTER SYSTEM ORGANIZATION**

**Objective Exam**

**Name: _____ Hall Ticket No.** | | | | | | A | | | | |

**Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.**

## I Choose the correct alternative:

1. To design a common bus system for 4 registers of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder? [ ]
   a) 2 to 4 Decoder b) 3 to 8 Decoder c) 4 to 16 Decoder d) 5 to 32 Decoder

2. If the address field of an instruction specifies the address of a memory location where effective address is available the instruction is [ ]
   a) Immediate Instruction b) Direct Instruction
   c) Indirect Instruction d) None of the above

3. The range of numbers that can be represented by *n*- bit integer, if the numbers are represented in signed magnitude format. [ ]
   a) $\pm (2^{n-1} - 1)$ b) $\pm (2^{n-1})$ c) $+ (2^{n-1})$ to $- (2^{n-1}-1)$ d) $- (2^{n-1}-1)$ to $+ (2^{n-1})$

4. To design a common bus system for 4 registers of 16-bits each, what is the size of each multiplexer? [ ]
   a) 2 x 1 MUX b) 4 x 1 MUX c) 8 x 1 MUX d) 16 x 1 MUX

5. The instruction code consists of one mode bit, three Opcode bits and 12 address bits. For an input – output instruction the combination of mode bit and Opcode bits will be [ ]
   a) 0111 b) 1111 c) 0110 d) 1110

6. The range of numbers that can be represented by *n* – bit register, if the numbers are represented in 2's complement format. [ ]
   a) $-(2^{n-1} - 1)$ to $+ (2^{n-1} - 1)$ b) $-(2^{n-1})$ to $+(2^{n-1} - 1)$
   c) $-(2^{n-1} - 1)$ to $+(2^{n-1})$ d) $-(2^{n-1})$ to $+ (2^{n-1})$

7. In a typical instruction format, the type of operation to be performed is specified by [ ]
   a) Mode field b) opcode field c) Address field d) None

8. The number of different logic operations that can be performed with '*n*' – binary variables is [ ]
   a) $2^n$ b) $2^{n+1}$ c) $2^{n-1}$ d) $2^{2^n}$

9. In which of the data transfer scheme, the computer monitors continuously the input and output flags, before performing data transfer? [ ]
   a) Interrupt initiated transfer b) Program controlled transfer
   c) DMA transfer d) None

**Cont...2**

**Code No: 07A5EC01** **Set No. 3**

10. Booth's multiplication algorithm specifies a procedure for multiplying two binary integers in . [ ]

a) Signed 2's complement b) Signed 1's complement
c) Signed magnitude d) None of the above

## II. Match the following:

| | | | |
|---|---|---|---|
| 11. | Autodecrement Mode | [ ] | a) Input output instructions |
| 12. | Data Register | [ ] | b) Memory reference instructions |
| 13. | Instruction Register | [ ] | c) Loops |
| 14. | S K I | [ ] | d) Holds the instruction code |
| 15. | I S Z | [ ] | e) Holds the data brought from memory |

## III. Fill in the blanks:

16. In a Array multiplier circuit with 'j' multiplier bits and 'k' multiplicand bits, the number of AND gates required are _____

17. In a memory stack, before every push operation, the stack pointer wll be _____

18. A divide overflow condition occurs, if the high order half bits of the dividend is _____

19. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

20. Arithmetic expressions can be evaluated more effectively by using _____Organization.

**-oOo-**

**Code No: 07A5EC01** **Set No. 4**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**III B.Tech I-Sem I Mid-Term Examinations, September– 2009**

**COMPUTER SYSTEM ORGANIZATION**

**Objective Exam**

**Name: _____ Hall Ticket No.** | | | | | | A | | | | |

**Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.**

## I Choose the correct alternative:

1. The range of numbers that can be represented by *n*- bit integer, if the numbers are represented in signed magnitude format. [ ]
   a) $\pm (2^{n-1} - 1)$ b) $\pm (2^{n-1})$ c) $+ (2^{n-1})$ to $- (2^{n-1}-1)$ d) $- (2^{n-1}-1)$ to $+ (2^{n-1})$

2. To design a common bus system for 4 registers of 16-bits each, what is the size of each multiplexer? [ ]
   a) 2 x 1 MUX b) 4 x 1 MUX c) 8 x 1 MUX d) 16 x 1 MUX

3. The instruction code consists of one mode bit, three Opcode bits and 12 address bits. For an input – output instruction the combination of mode bit and Opcode bits will be [ ]
   a) 0111 b) 1111 c) 0110 d) 1110

4. The range of numbers that can be represented by *n* – bit register, if the numbers are represented in 2's complement format. [ ]
   a) $-(2^{n-1} - 1)$ to $+ (2^{n-1} - 1)$ b) $-(2^{n-1})$ to $+(2^{n-1} - 1)$
   c) $-(2^{n-1} - 1)$ to $+(2^{n-1})$ d) $-(2^{n-1})$ to $+ (2^{n-1})$

5. In a typical instruction format, the type of operation to be performed is specified by [ ]
   a) Mode field b) opcode field c) Address field d) None

6. The number of different logic operations that can be performed with '*n*' – binary variables is [ ]
   a) $2^n$ b) $2^{n+1}$ c) $2^{n-1}$ d) $2^{2^n}$

7. In which of the data transfer scheme, the computer monitors continuously the input and output flags, before performing data transfer? [ ]
   a) Interrupt initiated transfer b) Program controlled transfer
   c) DMA transfer d) None

8. Booth's multiplication algorithm specifies a procedure for multiplying two binary integers in . [ ]
   a) Signed 2's complement b) Signed 1's complement
   c) Signed magnitude d) None of the above

9. To design a common bus system for 4 registers of 4-bits each, by using tristate buffers and a decoder, what is the size of the decoder? [ ]
   a) 2 to 4 Decoder b) 3 to 8 Decoder c) 4 to 16 Decoder d) 5 to 32 Decoder

**Cont...2**

**Code No: 07A5EC01** **Set No. 4**

10. If the address field of an instruction specifies the address of a memory location where effective address is available the instruction is [ ]
    a) Immediate Instruction b) Direct Instruction
    c) Indirect Instruction d) None of the above

## II. Match the following:

| | | | |
|---|---|---|---|
| 11. | Autodecrement Mode | [ ] | a) Input output instructions |
| 12. | Data Register | [ ] | b) Memory reference instructions |
| 13. | Instruction Register | [ ] | c) Loops |
| 14. | S K I | [ ] | d) Holds the instruction code |
| 15. | I S Z | [ ] | e) Holds the data brought from memory |

## III. Fill in the blanks:

16. A divide overflow condition occurs, if the high order half bits of the dividend is _____

17. The type of shift used to shift the contents of a register which contains a signed binary number is called _____

18. Arithmetic expressions can be evaluated more effectively by using _____Organization.

19. In a Array multiplier circuit with ‘j’ multiplier bits and ‘k’ multiplicand bits, the number of AND gates required are _____

20. In a memory stack, before every push operation, the stack pointer wll be _____

**-oOo-**