Code No: 07A4EC13 **Set No. I**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

II B.Tech II Sem. I Mid-Term Examinations, Feb. – 2009

COMPUTER ORGANIZATION

Objective Exam

Name:_____ **Hall Ticket No.** _____

Answer All Questions.All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. Convert the following binary number into decimal 101110 [ ]

   1.55 2.45 3.46 4.56

2. In _____ mode the content of the program counter is added to the address part of the instruction in order to obtain the effective address [ ]

   1. Relative address mode 2. Indexed address mode 3. Base address mode 4. Register mode

3. Description for EXCHANGE instruction [ ]
   1. M[EA]←AC 2. AC← M[EA], M[EA]← AC
   3. AC ←AC + M[EA] 4. all the above

4. In the _____ method, the digits are applied to a single BCD adder serially, while the bits of each coded digit are transferred in parallel. [ ]
   1. Parallel 2. Decimal arithmetic 3. Digit-serial bit-parallel 4. none

5. Obtain the 10's complement of the following 6-bit decimal number 100000 [ ]
   1. 999999 2. 899999 3. 900000 4. 100000

6. Two registers A&B, **A** holds 1010 & **B** holds 1100, determine A, after perform selective set operation [ ]
   1. 1110 2. 0111 3. 0110 4. 1001

7. In which symbol define the following micro operation M [AR] ←DR
   1.DRTAR 2. DRTAC 3. WRITE 4. READ

8. What is the description about following decimal arithmetic microoperation? $Q_L \leftarrow Q_L+1$ [ ]
   1.Increment Q_L register 2. Increment BCD number in Q_L

   3. Increment decimal number in Q_L 4. All the above

9. A _____ is an extra bit included with a binary message to make the total number of 1's either odd or even. [ ]
   1. Overflow bit 2. Parity bit 3. Insertion bit 4. Parity generator

10. Register Transfer language for Register indirect address mode [ ]
    1. AC←M [R1], R1←R1+1 2. AC←M [R1] 3. AC←R1 4. All the above

Cont…2

II Fill in the Blanks

11. The _____of an instruction is group bits that define operations.

12. The next address generator is also called as_____

13. The r's complement of an n-digit number N in base r is defined as ____.

14. Which memory is faster compare to RAM _____.

15. Expand RPN _____

III True or False

16. Personal computers which have found wide use in interactive design work. [True/False]

17. In Register mode the operands are in registers that reside within the CPU. [True/False]

18. A memory that is the part of the RAM memory is called as control memory. [True/False]

19. The partial product does not change when the multiplier bit is identical to the previous multiplier bit. [True/False]

20. A set of common instructions that can be used in a program many times is called a subroutine. [True/False]

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Code No: 07A4EC13 **Set No. 2**

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II B.Tech II Sem. I Mid-Term Examinations, Feb. – 2009

COMPUTER ORGANIZATION

Objective Exam

Name:_____ **Hall Ticket No.** _____

Answer All Questions.All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. Convert the hexadecimal number F3A7C2 to binary [ ]

   1.111101101101100010101001 2. 111111000101101101011110

   3. 111100111010011111000010 4. 111110011001100000010010

2. A digital computer has a common bus system for 16 registers of 32bit each. The bus constructed with multiplexers. How many selection inputs are there in each multiplexer? [ ]
   1. 3 2. 5 3. 2 4. 4

3. Description for ADD instruction [ ]
   1.M[EA]←AC 2. AC← M[EA], M[EA]← AC
   3.AC ←AC + M[EA] 4. all the above

4. A comparator circuit is needed to establish if [ ]
   1. A>B 2. A<B 3. A=B 4. all the above

5. The operand is specified in the instruction itself. [ ]
   1. Implied mode 2. Immediate mode 3. Register mode 4. Direct address mode

6. Perform the subtraction with the following unsigned decimal number by taking the 10's complement of the subtrahend 1200-250. [ ]
   1. 450 2. 750 3. 749 4. 449

7. A _____ is similar to ROM in concept that it uses AND , OR gates with internal electronic fuses. [ ]
   1. PLA 2. CAR 3. PLD 4. CCW

8. Which one is the data transfer instruction [ ]
   1. INC 2. NEG 3. XCH 4.SETC

9. In floating point division algorithm exponents are [ ]
   1. Multiplied 2. Subtracted 3. Added 4. Divide

Cont..2

10. Description of SPA instruction [ ]
1. Skip next instruction if AC positive 2. Skip next instruction if AC negative
3.Skip next instruction if AC zero 4. Skip next instruction if E is zero

II Fill the blanks

11. Expand EBCDIC _____

12. An _____is s a group of bits that instruct the computer to perform a specific operation.

13. The transformation from the instruction code bits to an address in control memory where the routine located is referred as _____.

14. The _____ method uses a decimal arithmetic unit composed of as many BCD adders as there are digits in the number.

15. Which memory is faster compare to RAM _____.

III True or False

16. Data manipulation instructions are those that perform arithmetic, logic and shift operation. [True/False]

17. selective clear operation is also called OR? [True/False]

18. A sequence of instruction is called as micro program? [True/False]

19. A call subroutine instruction consists of an operation code together with an address that specifies the beginning of the subroutine. [True/False]

20. The multiplicand is added to the partial product upon encountering the first least significant 1 in a string of 1's in the multiplier. [True/False]

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Code No: 07A4EC13 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

II B.Tech II Sem. I Mid-Term Examinations, Feb. – 2009

COMPUTER ORGANIZATION

Objective Exam

Name:_____ **Hall Ticket No.** _____

Answer All Questions.All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. A digital computer has a common bus system for 16 registers of 32bit each. The bus constructed with multiplexers. What size of multiplexer are needed? [ ]

   1. 32×1 2. 16×1 3. 2×1 4. 4×1

2. Perform the subtraction with the following unsigned decimal number by taking the 2's complement of the subtrahend 11010-1101. [ ]

   1. 00011 2. 11101 3. 00011 4.) 00010

3. The control logic is implemented with gates, flip-flops, decoders, and other digital circuits.[ ]

   1. Hardwired control 2. Microprogrammed 3. Control logic 4. None

4. Consider the arithmetic addition of two decimal digits in BCD, together with a possible carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than [ ]

   1. 18 2. 20 3.19 4. 17

5. The collection of all status bit conditions in the CPU is called as [ ]

   1. PLD 2. PSW 3. status bit 4. carry bit

6. Represent the decimal number $(+46.5)_{10}$ as a floating point binary number with 24-bits. The normalized fraction mantissa has 16-bits and the exponent has 8-bits. [ ]

   1. 010111010000000000001100 2. 001010100000000000001100
   3. 011111000000000000000011 4. 001100110000000000001010

7. Description for STORE instruction [ ]

   1. M[EA]←AC 2AC← M[EA], M[EA]← AC 3 AC ←AC + M[EA] 4. all the above

8. The multiplicand is _____ to the partial product upon encountering the first 0 in a string of 0's in the multiplier. [ ]

   1. Subtracted 2. Added 3. not changed 4. all the above

9. The application of work stations is [ ]

   1. Business Applications 2. Simulation 3. Interactive Design Work 4.All the above

10. RPN is also called as [ ]

    1. Infix Notation 2. Polish Notation 3. Prefix Notation 4. Postfix Notation

Cont…2

II Fill the blanks

11. Given a number N in base r having n digits, the (r-1)'s complement of N is defined as _____

12. For a memory unit with 4096 words we need ___bits to specify an address.

13. In array multiplier, for j multiplier bits and k multiplicand bits we need _____ AND gates and _____bit adders to produce a product of _____ bits.

14. In Micro programmed organization, the control information is stored in _____ .

15. _____ is a fast electronic calculating machine that accepts digitized input information, processes it according to a list of internally stored instructions and the resulting output information.

III Match the following

16.	Relative address	[ ]	P) AC←M[ADR]
17.	Indirect address	[ ]	Q) AC←M[PC+ADR]
18.	Index addressing	[ ]	R) AC←M[R1]
19.	Register indirect address	[ ]	S) AC←M[ADR+XR]
20.	Direct address	[ ]	T) AC←M[M[ADR]]

Code No: 07A4EC13 **Set No. 4**

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COMPUTER ORGANIZATION

Objective Exam

Name:_____ **Hall Ticket No.** _____

Answer All Questions.All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. Representation of floating point number is

   1.$m \times e^r$ 2. $m \times r^{e+1}$ 3. $m \times r^e$ 4.$m^{e+1} \times r$

2. _____ refer to the transfer of program control from a currently running program to another service program as result of external or internal generated request.

   1.Program Interrupt 2. Internal Interrupt 3. External Interrupt 4. Software Interrupt

3. The transformation from the instruction code bits to an address in control memory where the routine located is referred as _____

   1.Subroutine 2. Call Return 3. Mapping Process 4. Branch logic

4. The partial product does not change when the multiplier bit is identical to the previous multiplier bit.

   1. Subtracted 2. Added 3. Not changed 4. all the above

5. A digital computer has a common bus system for 16 registers of 32bit each. The bus constructed with multiplexers. How many multiplexer are there in the bus?

   1.4 2. 8 3. 16 4. 32

6. The number N is the actual number of instruction executions , the average number of basic steps need to executed one machine instruction is S, if clock rate is R cycles per second, the program execution time is

   A) T= R×S/N B) T= N×S/R C) T= N×R/S D) T= N×S/2R

7. The control data register holds the present microinstruction while the next address is computed and read from memory. The data register ids called as

   A) Index register B) Address register C) Pipeline register D) Temporary register

8. Description of SNA instruction
   A) Skip next instruction if AC positive B) Skip next instruction if AC negative
   C) Skip next instruction if AC zero D) Skip next instruction if E is zero

Cont….2

9. Convert the following octal number into decimal $(736.4)_8$
   1. $(745.5)_{10}$ 2. $(445.6)_{10}$ 3. $(478.5)_{10}$ 74. $(746.4)_{10}$

10. Two registers A&B, A holds 1010 and B holds 1100, determine A after perform Selective set operation.
    1. 1110 2. 0111 3. 0110 4. 1001

II. Fill in the blanks

11. xpand EEPROM _____

12. The _____holds the address of the next instruction to be read from memory after the current uction is executed.

13. An elementary operation performed on the information stored in one or more registers is referred as_____.

14. Effective Address = _____+ _____

15. In the _____ method, the digits are applied to a single BCD adder serially, while the bits of each coded digit are transferred in parallel.

III True or False

16. In Base register addressing mode the content of an index register is added to the address part of the instruction to obtain effective address? [True/False]

IV Match the Following

17)	ero –Address instruction	[ ]	P)AC←AC+M [D]
18)	Three - Address instruction	[ ]	Q) R2←M [D]
19	One- Address instruction	[ ]	R) R1←M [A] +M [B]
20)	Two- Address instruction	[ ]	S) M[X] ←TOS