Code No: 07A5EC01 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. I Sem., II Mid-Term Examinations, November – 2010

COMPUTER SYSTEM ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. The Static RAM consists of [ ]
   a. Capacitors b. Internal Flip Flops c. Internal Caches d. Filters

2. If Cache Access time is 100ns, Memory access time is 1000ns, if the hit percentage is 100 %, what is the Average access time [ ]
   a. 100 b. 1000 c. 1100 d. 10

3. The technique of Segmentation suffers which fragmentation [ ]
   a. Internal b. External c. both Internal and External d. Neither Internal nor External

4. Which is not a Flynn's classification [ ]
   a. SISD b. SIMD c. MISD d. NONE

5. Each processor element in a _____system has its own private local memory [ ]
   a. loosely coupled b. time shared c. tightly coupled d. multistage

6. The decoder used for decoding 512 x 8 ROM consists of how many input lines [ ]
   a. 512 b. 8 c. 9 d. 520

7. In Cache, the data stored is [ ]
   a. Most frequently used b. Least frequently used c. Never used d. Segment with large data

8. The command used to activate the peripheral and to inform it what to do is [ ]
   a. Control command b. Status command c. Data output command d. Data input command

9. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
   a.Cost per bit Increases b.Speed Increases
   c.Access Time Decreases d.Cost per bit decreases

10 DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
   a. polling b. burst transfer c. daisy chaining d. cycle stealing

Cont....2

II Fill in the Blanks

11. Pipelining is _____

12. MIMD stands _____.

13. In Daisy chaining, device with highest priority is in _____ position

14. A _____pipeline divides an arithmetic operation into suboperations for execution in the pipeline segments.

15. _____mapping uses different address space for Memory and I/O

16. Continuously monitoring I/O devices is done in _____ I/O

17. Total operations performed going through all the segments in the pipeline is called as_____

18. The sequence of instructions read from memory constitutes _____

19. SIMD stands _____.

20. _____ determines the termination of a vector instruction.

-oOo-

Code No: 07A5EC01 **Set No. 2**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. I Sem., II Mid-Term Examinations, November – 2010

COMPUTER SYSTEM ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. Which is not a Flynn's classification [ ]
   a. SISD b. SIMD c. MISD d. NONE

2. Each processor element in a _____system has its own private local memory [ ]
   a. loosely coupled b. time shared c. tightly coupled d. multistage

3. The decoder used for decoding 512 x 8 ROM consists of how many input lines [ ]
   a. 512 b. 8 c. 9 d. 520

4. In Cache, the data stored is [ ]
   a. Most frequently used b. Least frequently used c. Never used d. Segment with large data

5. The command used to activate the peripheral and to inform it what to do is [ ]
   a. Control command b. Status command c. Data output command d. Data input command

6. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
   a. Cost per bit Increases b. Speed Increases
   c. Access Time Decreases d. Cost per bit decreases

7 DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
   a. polling b. burst transfer c. daisy chaining d. cycle stealing

8. The Static RAM consists of [ ]
   a. Capacitors b. Internal Flip Flops c. Internal Caches d. Filters

9. If Cache Access time is 100ns, Memory access time is 1000ns, if the hit percentage is 100 %, what is the Average access time [ ]
   a. 100 b. 1000 c. 1100 d. 10

10. The technique of Segmentation suffers which fragmentation [ ]
    a. Internal b. External c. both Internal and External d. Neither Internal nor External

Cont....2

II Fill in the Blanks:

11. A _____ pipeline divides an arithmetic operation into suboperations for execution in the pipeline segments.

12. _____mapping uses different address space for Memory and I/O

13. Continuously monitoring I/O devices is done in _____ I/O

14. Total operations performed going through all the segments in the pipeline is called as_____

15. The sequence of instructions read from memory constitutes _____

16. SIMD stands _____.

17. _____ determines the termination of a vector instruction.

18. Pipelining is _____

19. MIMD stands _____.

20. In Daisy chaining, device with highest priority is in _____ position

-oOo-

Code No: 07A5EC01 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. I Sem., II Mid-Term Examinations, November – 2010

COMPUTER SYSTEM ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. The decoder used for decoding 512 x 8 ROM consists of how many input lines [ ]
   a. 512 b. 8 c. 9 d. 520

2. In Cache, the data stored is [ ]
   a. Most frequently used b. Least frequently used c. Never used d. Segment with large data

3. The command used to activate the peripheral and to inform it what to do is [ ]
   a. Control command b. Status command c. Data output command d. Data input command

4. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
   a. Cost per bit Increases b. Speed Increases
   c. Access Time Decreases d. Cost per bit decreases

5 DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
   a. polling b. burst transfer c. daisy chaining d. cycle stealing

6. The Static RAM consists of [ ]
   a. Capacitors b. Internal Flip Flops c. Internal Caches d. Filters

7. If Cache Access time is 100ns, Memory access time is 1000ns, if the hit percentage is 100 %, what is the Average access time [ ]
   a. 100 b. 1000 c. 1100 d. 10

8. The technique of Segmentation suffers which fragmentation [ ]
   a. Internal b. External c. both Internal and External d. Neither Internal nor External

9. Which is not a Flynn's classification [ ]
   a. SISD b. SIMD c. MISD d. NONE

10. Each processor element in a _____system has its own private local memory [ ]
    a. loosely coupled b. time shared c. tightly coupled d. multistage

Cont....2

II Fill in the Blanks:

11. Continuously monitoring I/O devices is done in _____ I/O

12. Total operations performed going through all the segments in the pipeline is called as_____

13. The sequence of instructions read from memory constitutes _____

14. SIMD stands _____.

15. _____ determines the termination of a vector instruction.

16. Pipelining is _____

17. MIMD stands _____.

18. In Daisy chaining, device with highest priority is in _____ position

19. A _____ pipeline divides an arithmetic operation into suboperations for execution in the pipeline segments.

20. _____mapping uses different address space for Memory and I/O

-oOo-

Code No: 07A5EC01 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. I Sem., II Mid-Term Examinations, November – 2010

COMPUTER SYSTEM ORGANIZATION

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 20.

I Choose the correct alternative:

1. The command used to activate the peripheral and to inform it what to do is [ ]
   a. Control command b. Status command c. Data output command d. Data input command

2. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
   a. Cost per bit Increases b. Speed Increases
   c. Access Time Decreases d.Cost per bit decreases

3 DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
   a. polling b. burst transfer c. daisy chaining d. cycle stealing

4. The Static RAM consists of [ ]
   a. Capacitors b. Internal Flip Flops c. Internal Caches d. Filters

5. If Cache Access time is 100ns, Memory access time is 1000ns, if the hit percentage is 100 %, what is the Average access time [ ]
   a. 100 b. 1000 c. 1100 d. 10

6. The technique of Segmentation suffers which fragmentation [ ]
   a. Internal b. External c. both Internal and External d. Neither Internal nor External

7. Which is not a Flynn's classification [ ]
   a. SISD b. SIMD c. MISD d. NONE

8. Each processor element in a _____system has its own private local memory [ ]
   a. loosely coupled b. time shared c. tightly coupled d. multistage

9. The decoder used for decoding 512 x 8 ROM consists of how many input lines [ ]
   a. 512 b. 8 c. 9 d. 520

10. In Cache, the data stored is [ ]
    a. Most frequently used b. Least frequently used c. Never used d. Segment with large data

Cont....2

II Fill in the Blanks:

11. The sequence of instructions read from memory constitutes _____

12. SIMD stands _____.

13. _____ determines the termination of a vector instruction.

14. Pipelining is _____

15. MIMD stands _____.

16. In Daisy chaining, device with highest priority is in _____ position

17. A _____ pipeline divides an arithmetic operation into suboperations for execution in the pipeline segments.

18. _____mapping uses different address space for Memory and I/O

19. Continuously monitoring I/O devices is done in _____ I/O

20. Total operations performed going through all the segments in the pipeline is called as_____

-oOo-