Code No: 07A5EC01 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., II Mid-Term Examinations, November– 2009
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____Hall Ticket No. | | | | | | **A** | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I. Choose the correct alternative:

1. For a magnetic disk, the access is _____ [ ]
(a) Sequential access (b) Random access (c) direct access (d) both a &b

2. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
(a)Cost per bit Increases (b)Speed Increases (c)Access Time Decreases (d)Cost per bit decreases

3. In the following, which uses separate controller for data transfer? [ ]
(a) Programmed I/O (b) DMA (c) Memory mapped I/O (d) Interrupt interrupted I/O

4. DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
(a) polling (b) burst transfer (c) daisy chaining (d) cycle stealing

5. A pipeline contains_____ [ ]
(a) segments (b) computational circuit (c) both a&b (d) none

6. Which is not a Flynn's classification? [ ]
(a) SISD (b) SIMD (c) MISD (d) NONE

7. Time shared common bus organization includes a single common bus shared by _____ processors. [ ]
(a) single (b) two (c) three (d) multiple

8. Each processor element in a system has its own private local memory [ ]
(a) loosely coupled (b)time shared (c)tightly coupled (d)multistage

9.The processor in a shared memory multiprocessor system request access to common memory through [ ]
(a) synchronized bus (b) internal bus (c)system bus (d) a synchronous bus

10. The inter process communication mechanism used in loosely coupled system is _____ [ ]
(a) Message queues (b) FIFO (c) pipes (d) shared memory

Cont…2

Code No: 07A5EC01 **Set No. 1**

II. Fill in the Blanks:

11. The rate at which Serial information is transmitted and is equivalent to the data transfer in bits per second is_____.

12. Pipelining is _____.

13. _____is a circuit that detects instructions who Resource operands are destination so instructions further up in the pipeline.

14. MIMD stands _____.

15. The bus controller that monitors the cache coherence problem is referred as _____

16.A memory scheme is if the value returned on a load instruction is always the value given by the latest store instruction with the same address_____.

17. The sequence of instructions read from memory constitutes _____

18. SIMD stands _____.

19. A system supporting interconnection structure of more than one processor is referred as _____.

20. _____ determines the termination of a vector instruction.

-oOo-

Code No: 07A5EC01 **Set No. 2**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., II Mid-Term Examinations, November– 2009
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | **A** | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I. Choose the correct alternative:

1. DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
(a) polling (b) burst transfer (c) daisy chaining (d) cycle stealing

2. A pipeline contains_____ [ ]
(a) segments (b) computational circuit (c) both a&b (d) none

3. Which is not a Flynn's classification? [ ]
(a) SISD (b) SIMD (c) MISD (d) NONE

4. Time shared common bus organization includes a single common bus shared by _____ processors. [ ]
(a) single (b) two (c) three (d) multiple

5. Each processor element in a system has its own private local memory [ ]
(a) loosely coupled (b)time shared (c)tightly coupled (d)multistage

6.The processor in a shared memory multiprocessor system request access to common memory through [ ]
(a) synchronized bus (b) internal bus (c)system bus (d) a synchronous bus

7. The inter process communication mechanism used in loosely coupled system is _____ [ ]
(a) Message queues (b) FIFO (c) pipes (d) shared memory

8. For a magnetic disk, the access is _____ [ ]
(a) Sequential access (b) Random access (c) direct access (d) both a &b

9. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
(a)Cost per bit Increases (b)Speed Increases (c)Access Time Decreases (d)Cost per bit decreases

10. In the following, which uses separate controller for data transfer? [ ]
(a) Programmed I/O (b) DMA (c) Memory mapped I/O (d) Interrupt interrupted I/O

Cont…2

Code No: 07A5EC01 **Set No. 2**

II. Fill in the Blanks:

11. MIMD stands _____.

12. The bus controller that monitors the cache coherence problem is referred as _____

13.A memory scheme is if the value returned on a load instruction is always the value given by the latest store instruction with the same address_____.

14. The sequence of instructions read from memory constitutes _____

15. SIMD stands _____.

16. A system supporting interconnection structure of more than one processor is referred as _____.

17. _____ determines the termination of a vector instruction.

18. The rate at which Serial information is transmitted and is equivalent to the data transfer in bits per second is_____.

19. Pipelining is _____.

20. _____is a circuit that detects instructions who Resource operands are destination so instructions further up in the pipeline.

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Code No: 07A5EC01 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., II Mid-Term Examinations, November– 2009
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | **A** | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I. Choose the correct alternative:

1. Which is not a Flynn's classification? [ ]
(a) SISD (b) SIMD (c) MISD (d) NONE

2. Time shared common bus organization includes a single common bus shared by _____ processors. [ ]
(a) single (b) two (c) three (d) multiple

3. Each processor element in a system has its own private local memory [ ]
(a) loosely coupled (b)time shared (c)tightly coupled (d)multistage

4.The processor in a shared memory multiprocessor system request access to common memory through [ ]
(a) synchronized bus (b) internal bus (c)system bus (d) a synchronous bus

5. The inter process communication mechanism used in loosely coupled system is _____ [ ]
(a) Message queues (b) FIFO (c) pipes (d) shared memory

6. For a magnetic disk, the access is _____ [ ]
(a) Sequential access (b) Random access (c) direct access (d) both a &b

7. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
(a)Cost per bit Increases (b)Speed Increases (c)Access Time Decreases (d)Cost per bit decreases

8. In the following, which uses separate controller for data transfer? [ ]
(a) Programmed I/O (b) DMA (c) Memory mapped I/O (d) Interrupt interrupted I/O

9. DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
(a) polling (b) burst transfer (c) daisy chaining (d) cycle stealing

10. A pipeline contains_____ [ ]
(a) segments (b) computational circuit (c) both a&b (d) none

Cont…2

Code No: 07A5EC01 **Set No. 3**

II. Fill in the Blanks:

11.A memory scheme is if the value returned on a load instruction is always the value given by the latest store instruction with the same address_____.

12. The sequence of instructions read from memory constitutes _____.

13. SIMD stands _____.

14. A system supporting interconnection structure of more than one processor is referred as _____.

15. _____ determines the termination of a vector instruction.

16. The rate at which Serial information is transmitted and is equivalent to the data transfer in bits per second is_____.

17. Pipelining is _____.

18. _____is a circuit that detects instructions who Resource operands are destination so instructions further up in the pipeline.

19. MIMD stands _____.

20. The bus controller that monitors the cache coherence problem is referred as _____

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Code No: 07A5EC01 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
III B.Tech. I Sem., II Mid-Term Examinations, November– 2009
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____Hall Ticket No. | | | | | | **A** | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 20.

I. Choose the correct alternative:

1. Each processor element in a system has its own private local memory [ ]
(a) loosely coupled (b)time shared (c)tightly coupled (d)multistage

2.The processor in a shared memory multiprocessor system request access to common memory through [ ]
(a) synchronized bus (b) internal bus (c)system bus (d) a synchronous bus

3. The inter process communication mechanism used in loosely coupled system is _____ [ ]
(a) Message queues (b) FIFO (c) pipes (d) shared memory

4. For a magnetic disk, the access is _____ [ ]
(a) Sequential access (b) Random access (c) direct access (d) both a &b

5. In the Memory Hierarchy, top to bottom (Registers to Tape) [ ]
(a)Cost per bit Increases (b)Speed Increases (c)Access Time Decreases (d)Cost per bit decreases

6. In the following, which uses separate controller for data transfer? [ ]
(a) Programmed I/O (b) DMA (c) Memory mapped I/O (d) Interrupt interrupted I/O

7. DMA controller transfer one data word at a time and transfers the control of the bus to CPU. This is _____ [ ]
(a) polling (b) burst transfer (c) daisy chaining (d) cycle stealing

8. A pipeline contains_____ [ ]
(a) segments (b) computational circuit (c) both a&b (d) none

9. Which is not a Flynn's classification? [ ]
(a) SISD (b) SIMD (c) MISD (d) NONE

10. Time shared common bus organization includes a single common bus shared by _____ processors. [ ]
(a) single (b) two (c) three (d) multiple

Cont…2

Code No: 07A5EC01 **Set No. 4**

II. Fill in the Blanks:

11. SIMD stands _____.

12. A system supporting interconnection structure of more than one processor is referred as _____.

13. _____ determines the termination of a vector instruction.

14. The rate at which Serial information is transmitted and is equivalent to the data transfer in bits per second is_____.

15. Pipelining is _____.

16. _____is a circuit that detects instructions who Resource operands are destination so instructions further up in the pipeline.

17. MIMD stands _____.

18. The bus controller that monitors the cache coherence problem is referred as _____

19.A memory scheme is if the value returned on a load instruction is always the value given by the latest store instruction with the same address_____.

20. The sequence of instructions read from memory constitutes _____

-oOo-